

Do czego służą studnie, druty, kropki kwantowe?



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Jak TO działa? <http://www.fuw.edu.pl/~szczytko/>



Google: Jacek Szczytko
 Login: student
 Hasło: *****

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Półprzewodniki

II	III	IV	V	VI
Be	B	C	N	O
Mg	Al	Si	P	S
Zn	Ga	Ge	As	Se
Cd	In	Sn	Sb	Te

Nośniki:

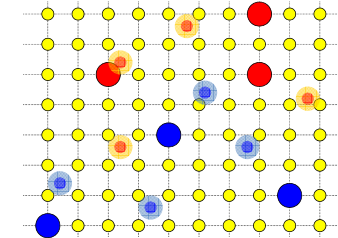
dziury + ●

elektrony - ●

Domieszki:

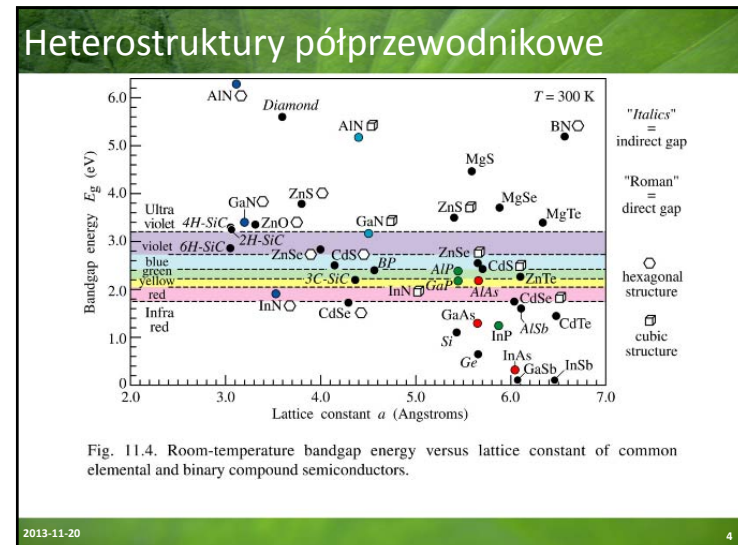
● Akceptory (typ p)

● Donory (typ n)



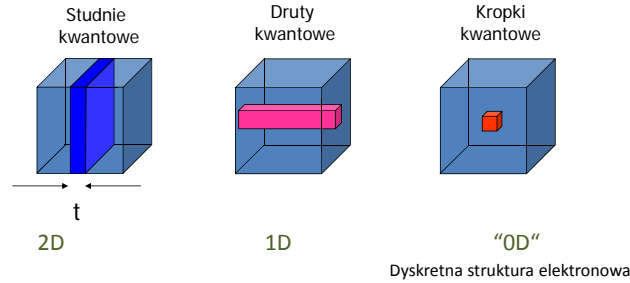
Grupa IV: diament, Si, Ge
Grupy III-V: GaAs, AlAs, InSb, InAs...
Grupy II-VI: ZnSe, CdTe, ZnO, SdS...

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Struktury niskowymiarowe

Low-dimensional Semiconductor Systems



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Jak się robi heterostruktury?

Liquid-phase (LPE)

wzrost z fazy ciekłej na podłożu w temperaturach niższych od temperatury topnienia hodowanego materiału. Półprzewodnik jest rozpuszczony w cieczy innego materiału, wzrost w warunkach bliskich równowagi roztworu i depozycji; prędkości wzrostu 0.1 to 1 μm/min.

Vapor-phase (VPE, CVD)

wzrost z fazy gazowej dzięki reakcjom chemicznym prekursorów na powierzchni, często dzielony ze względu na źródłowe gazy na wodorkową VPE i metalorganiczną VPE (MOCVD); prędkości wzrostu >10 -20 nm/min.

Molecular-beam (MBE)

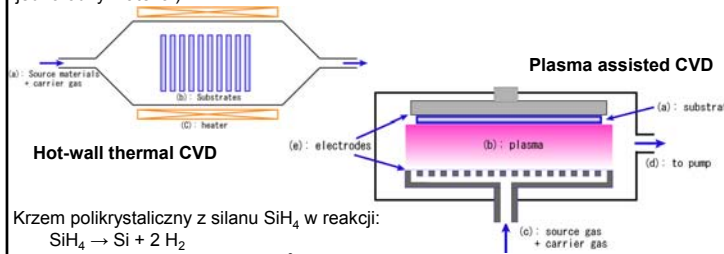
Materiał źródłowy podgrzewany w komórkach produkuje strumień cząstek. W wysokiej próżni (10⁻⁸ Pa) cząsteczki docierają do podłoża i osadzają się na nim; prędkości wzrostu < 1 monowarstwa/s (1 μm/h).

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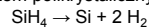
6

Jak się robi heterostruktury?

Chemical Vapor Deposition (CVD) – proces chemiczny, w którym do obszaru, gdzie znajduje się podłoże doprowadzone są jeden lub więcej prekursorów reagujących z podłożem w wyniku czego powstaje pożądany materiał. Jest to często stowarzyszone z lotnymi produktami, które usuwane są strumieniem gazu przepływającego przez komorę. (Si, SiC, SiN, dielektryki, diament syntetyczny).
Proces może przebiegać w ciśnieniu normalnym lub obniżonym (wolniej, bardziej jednorodny materiał).



Krzem polikrystaliczny z silanu SiH₄ w reakcji:



LPCVD, temperatura 600 and 650°C, ciśnienie 25 -150 Pa, prędkość wzrostu 10 -20 nm/min.

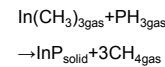
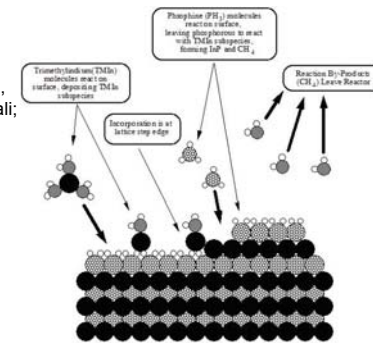
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Jak się robi heterostruktury?

Metalorganic chemical vapor deposition (MOCVD)

– proces CVD reakcji chemicznych na powierzchni z zastosowaniem związków organicznych, metalorganicznych oraz wodorków metali; zachodzi z gazu pod obniżonym ciśnieniem (2-100 kPa); np. InP z trymetylu indu In(CH₃)₃ i fosfinu PH₃; główna metoda dla produkcji diod, diod laserowych, złącz fotowoltaicznych



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Jak się robi heterostruktury?

Metalorganic chemical vapor deposition (MOCVD) –

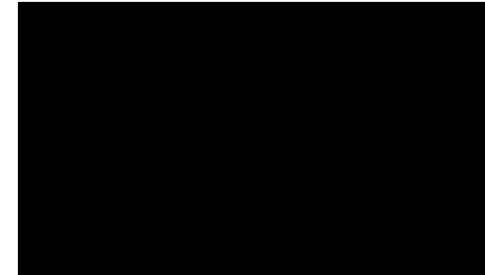


TurboDisc MaxBright M GaN MOCVD Multi-Reactor System

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Jak się robi heterostruktury?



TurboDisc K465i Animation

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Jak się robi heterostruktury?

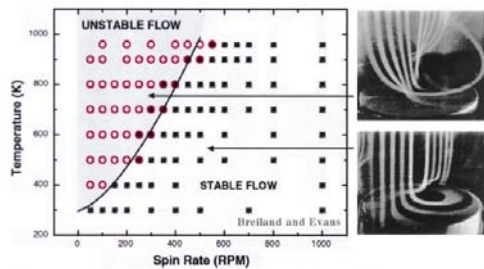


Fig. 10. Plot of the results of flow visualization experiments for a heated, spinning disk. Asterisks indicate that the flow is stable with a steady-state, fixed pattern, as illustrated in the lower right photo. Open circles indicate unstable, time-dependent flow patterns, as illustrated in the upper right photo. The transition from unstable to stable flow is characterized by the mixed convection parameter (MCP) defined by Eq. (27).

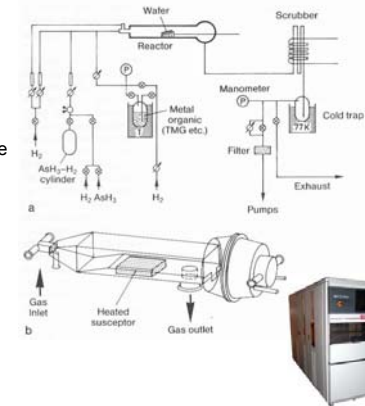
Organometallic vapor phase epitaxy (OMVPE) Materials Science and Engineering, R24 (1999) 241-274

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Jak się robi heterostruktury?

Podłoże umieszczone na podgrzewanym piecyku indukcyjnym RF graficie wewnątrz komory reakcyjnej. Typowe temperatury 500°C do 800°C. Wzrost w atmosferze wodoru i ciśnieniu 100 - 700 Torr. Prekursory rozkładają się w kontakcie z gorącym podłożem i tworzą warstwę. Prekursory grupy V: AsH₃ (arsin), PH₃ (fosfin), grupy III: Ga(CH₃)₃ Trimethylgallium (TMG), Al(CH₃)₃ Trimethylaluminium (TMA), In(CH₃)₃ trimethylindium (TMI), Domieszkowanie: SiH₄ Silane, Zn(C₂H₅)₂ Diethylzinc (DEZ).



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Jak się robi heterostruktury?

Reaktor Metal-Organic Chemical Vapour Epitaxy (MOCVD) w Zakładzie Fizyki Ciała Stałego



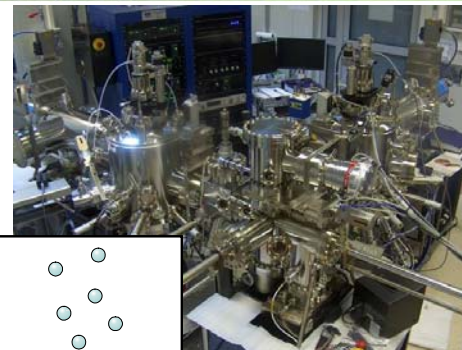
Aixtron CCS 3x2

Heterostruktury GaInSb, AlGaInAs and AlGaIn.

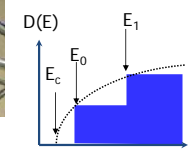
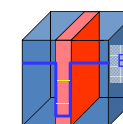
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Jak się robi heterostruktury?

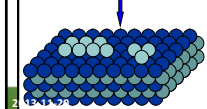


Quantum Well



2D

Hubert J. Krenner



MBE → Osadzanie z atomową precyzją warstw o różnym składzie lub domieszkowaniu

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Jak się robi heterostruktury?

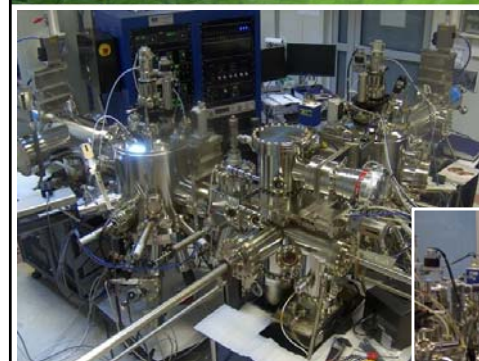


MBE na Wydziale Fizyki UW

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Jak się robi heterostruktury?



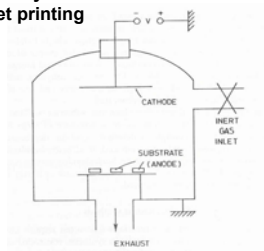
MBE na Wydziale Fizyki UW

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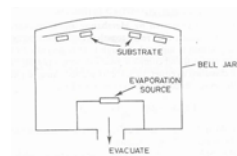
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Jak się robi heterostrukury?

- W dzisiejszych dla otrzymywania cienkich warstw czasach często stosuje się również tanie technologie:
- elektrochemiczne (elektrolityczne nakładanie metali, elektrolityczne utlenianie),
 - sputteringowe
 - naparowywania warstw.
 - ink-jet printing



Sputtering katodowy
obniżone ciśnienie 10^{-1} - 10^{-2} Torr gazu obojętnego przy napięciu kilkunastu kV jony dodatnie wybijają materiał katody i osadzają go na m.in. materiale podłożowym



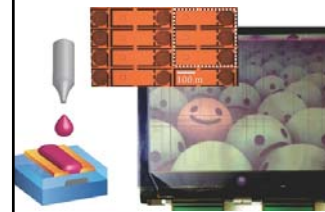
Naparowywanie warstw
w próżni $<10^{-6}$ Torr materiał źródłowy jest zamieniany w fazę gazową przez podgrzanie lub bombardowanie i deponuje się na m.in. materiale podłożowym

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Jak się robi heterostrukury?

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- elektrochemiczne (elektrolityczne nakładanie metali, elektrolityczne utlenianie),
 - sputteringowe
 - naparowywania warstw.
 - ink-jet printing



Reliable and Uniform Thin-Film Transistor Arrays Based on Inkjet-Printed Polymer Semiconductors for Full Color Reflective Displays
Jiyoul Lee, Do Hwan Kim, Joo-Young Kim, Byungwook Yoo, Jong Won Chung, Jeong-Il Park, Bang-Lin Lee, Ji Young Jung, Joon Seok Park, Bomwon Kos, Seonpil Im, Jung Wook Kim, Byungkwon Song, Myung-Hoon Jung, Jir Eun Jung, Yong Won Jin, and Sang-Yoon Lee

polymer light-emitting-diode (PLED)

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Jak się robi heterostrukury?

- ink-jet printing

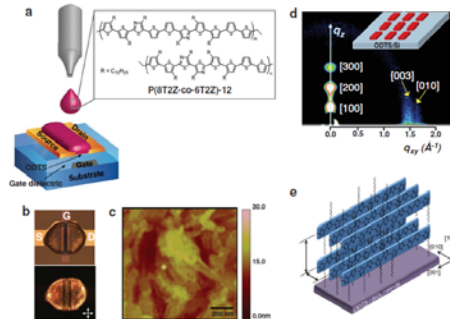


Figure 1. a) Inkjet printing scheme of OTFT and molecular design for polymer semiconductor P[BTZZ-co-6TZZ]-12 with charge-transfer moieties used in this system. b) Optical vs. polarized microscopy of the inkjet-printed OTFT device. c) Atomic force microscopy image of active channel area of the printed OTFT (right). d) Molecular packing and orientation of inkjet-printed P[BTZZ-co-6TZZ]-12 films characterized by 2D-GIXD. Film was post-annealed at 150 °C on ODS treated SiO₂ gate dielectrics. e) Schematic illustration of molecular ordering in inkjet-printed P[BTZZ-co-6TZZ]-12 polymer semiconductor film.

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Jak się robi heterostrukury?

- ink-jet printing

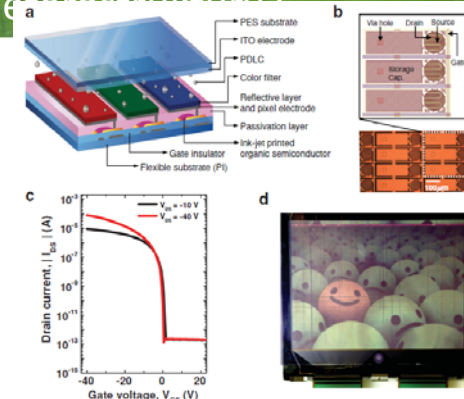


Figure 4. a) Schematic 3-dimensional view of one PDLC display pixel including OTFT drivers for red, green, and blue color display. b) Pixel array photos taken from optical microscopy, along with detailed scheme of one pixel that contains storage capacitors and three TFTs with interdigitized channels. c) Our TFTs display decent transfer characteristics with high mobility even after completion of all the backplane processes. d) 4.8-inch QVGA color reflective PDLC Display driven by inkjet-printed OTFTs.

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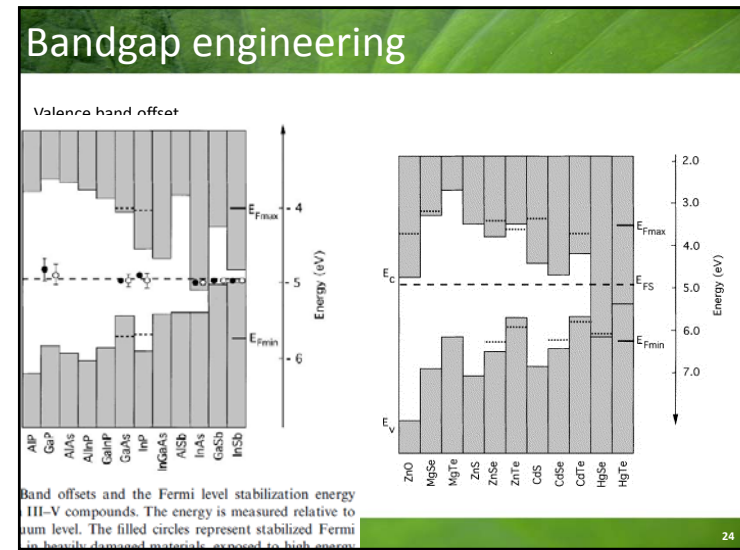
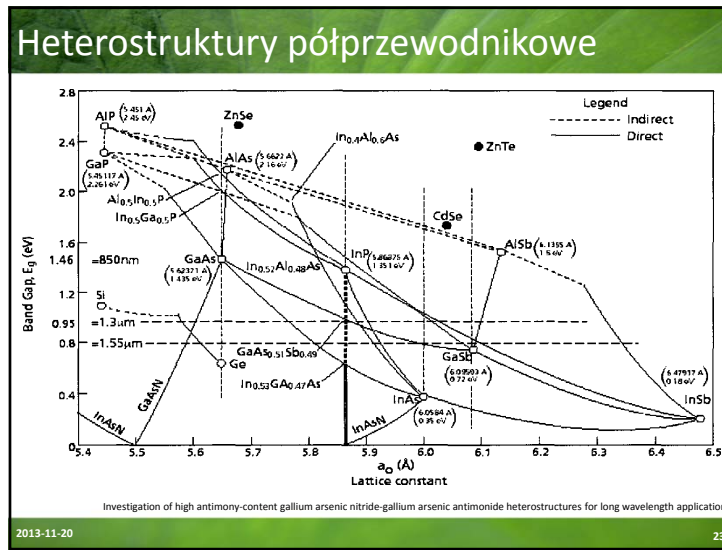
20

Jak

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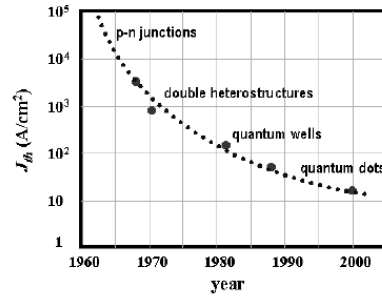
Jak

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Druty kwantowe

Figure 8 The trend of the reduction of semiconductor laser threshold



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Nanotechnologia

CO?

- Studnie, druty, kropki

JAK?

- Top-down, czyli (nano)technologia
- Bottom-up, czyli samoorganizacja

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Nanotechnologia

CO?

- Studnie, druty, kropki

JAK?

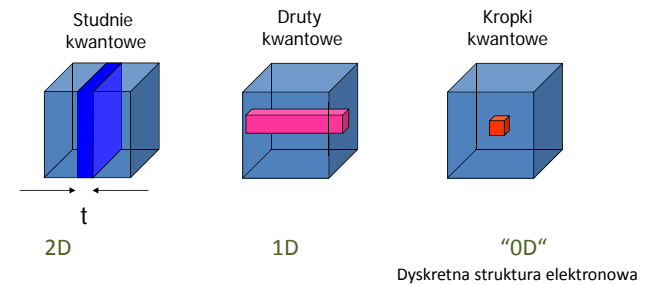
- Top-down, czyli (nano)technologia
- Bottom-up, czyli samoorganizacja

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Struktury niskowymiarowe

Low-dimensional Semiconductor Systems



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Struktury niskowymiarowe

Low-dimensional Semiconductor Systems

Studnie kwantowe

2D

Druty kwantowe

1D

Kropki kwantowe

"0D"

Dyskretna struktura elektronowa

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Studnia Kwantowa

AlGaAs

+

GaAs

+

AlGaAs

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Studnia Kwantowa

AlGaAs

+

GaAs

+

AlGaAs

=

AlGaAs GaAs AlGaAs

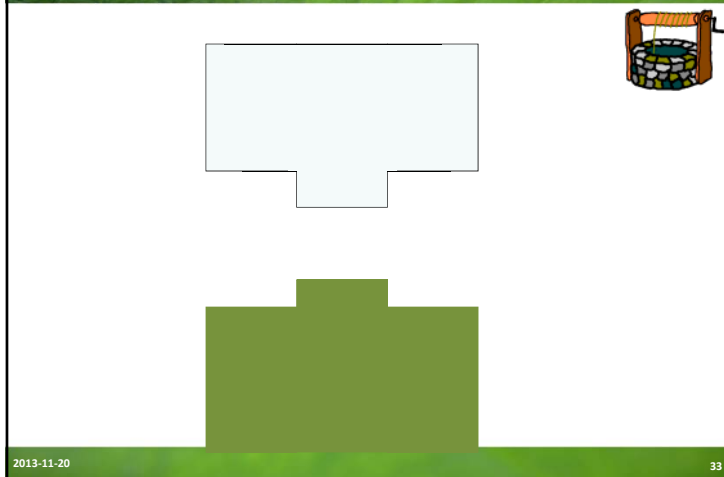
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Studnia Kwantowa

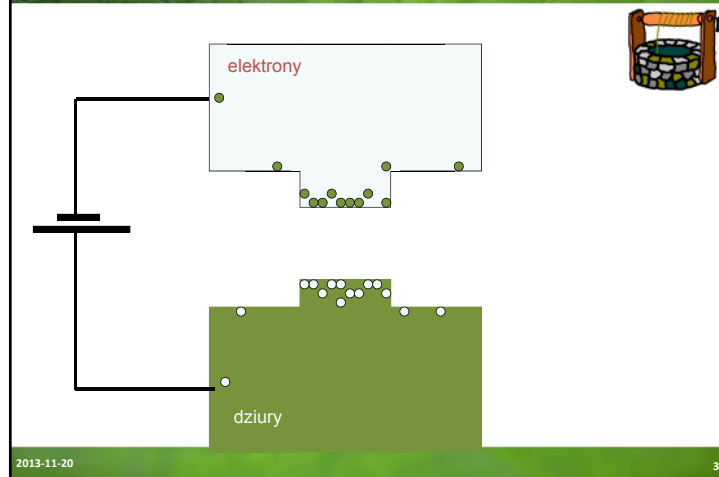
AlGaAs GaAs AlGaAs

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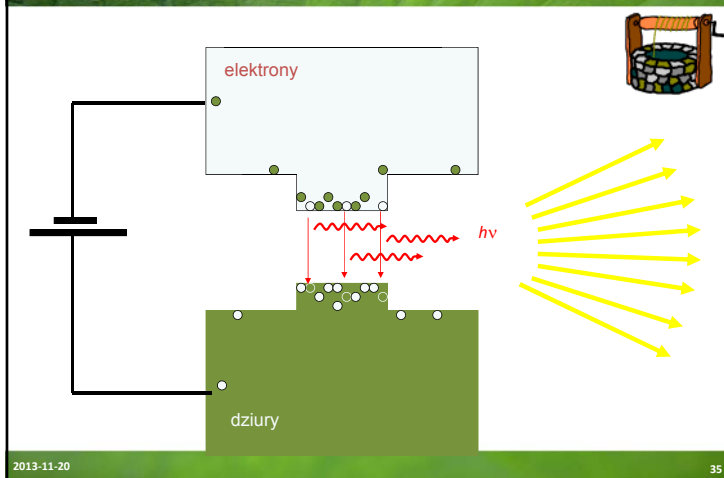
Studnia Kwantowa



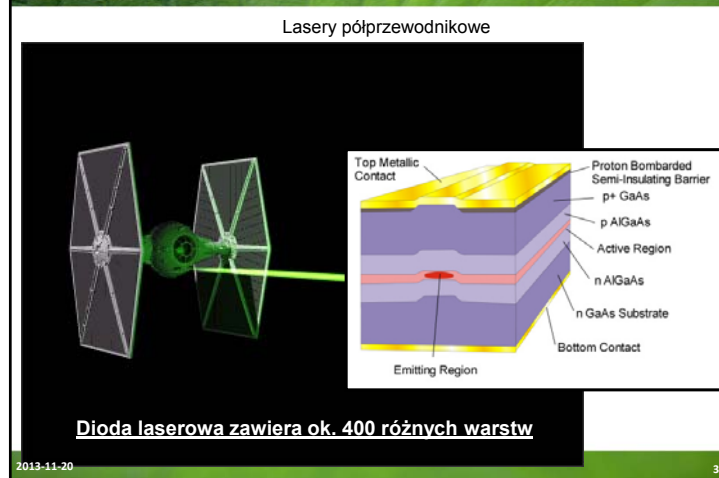
Studnia Kwantowa



Studnia Kwantowa

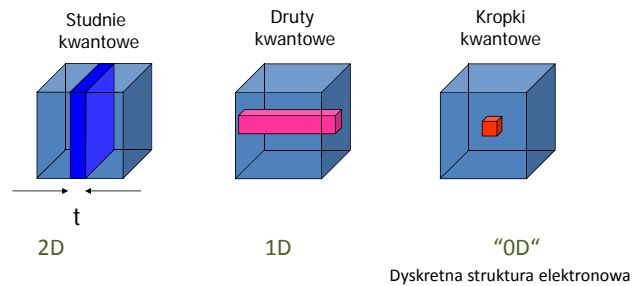


Studnia Kwantowa



Struktury niskowymiarowe

Low-dimensional Semiconductor Systems



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Studnia kwantowa

Więcej: <http://britneyspears.ac/lasers.htm>



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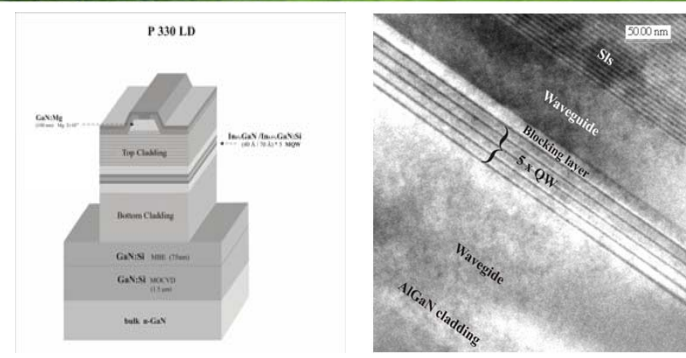
38



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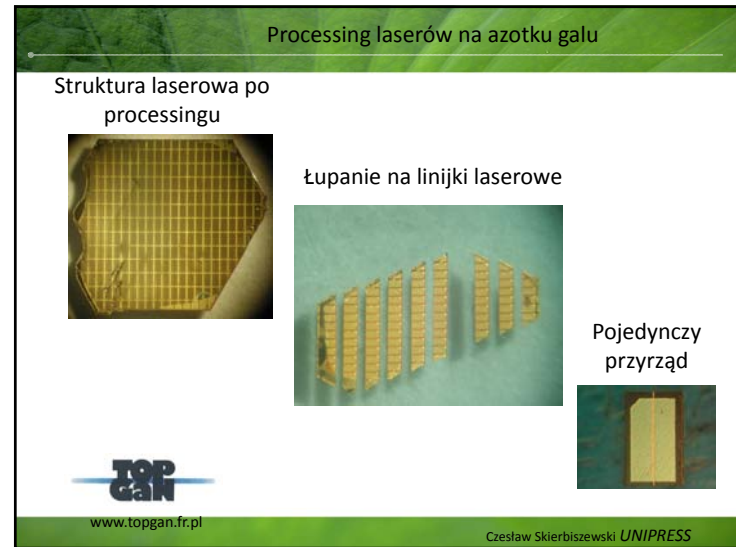
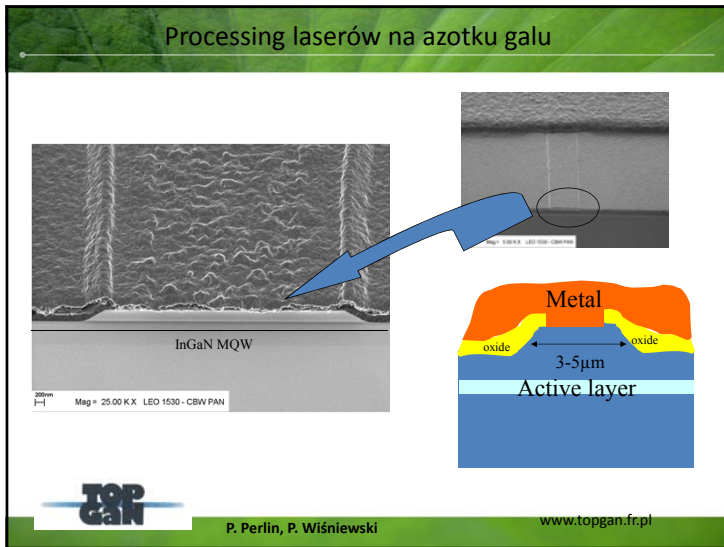
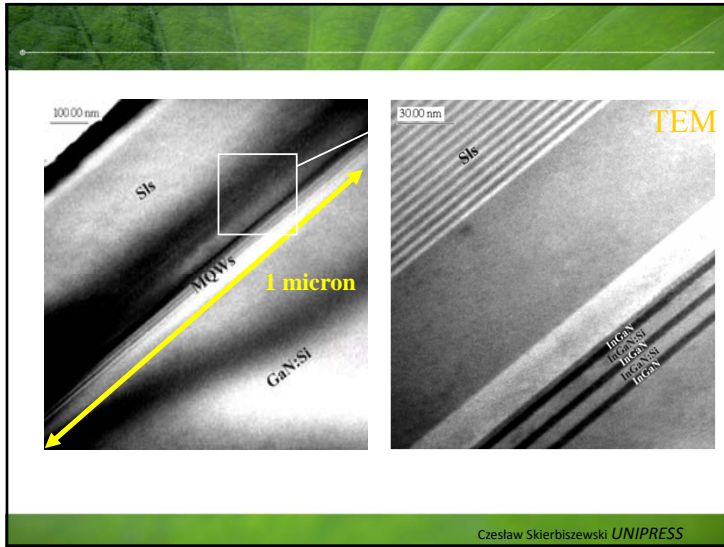
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Dioda laserowa wykonana metodą MBE



TEM

Czesław Skierbiszewski UNIPRESS



Lasery półprzewodnikowe są bardzo małe

Szerokość kostki = 0.3 mm

Długość lasera = 0.5 - 1 mm

Szerokość lasera = 0.001 – 0.02 mm !! (1 μm - 20 μm)

5 mikronów

IWC PAN, UNIPRESS

Montaż laserów – wersja impulsowa

www.topgan.fr.pl

Czesław Skierbiszewski UNIPRESS

Struktury niskowymiarowe

Low-dimensional Semiconductor Systems

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“0D”
Dyskretna struktura elektronowa

Hubert J. Keenler

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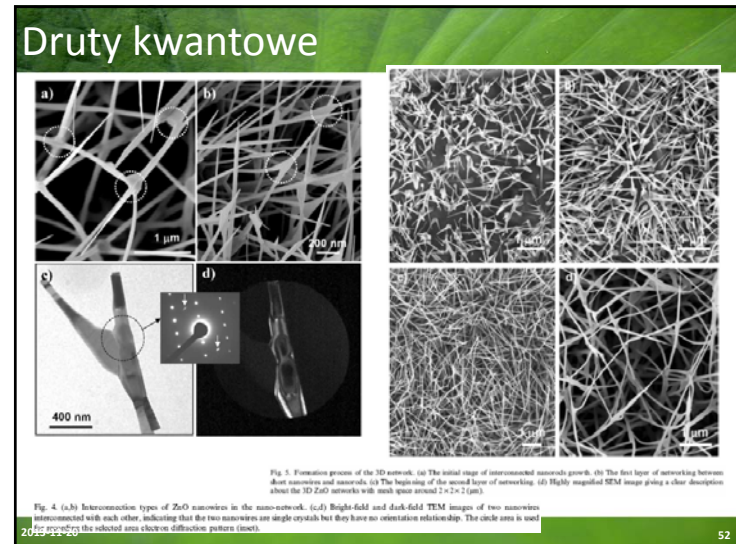
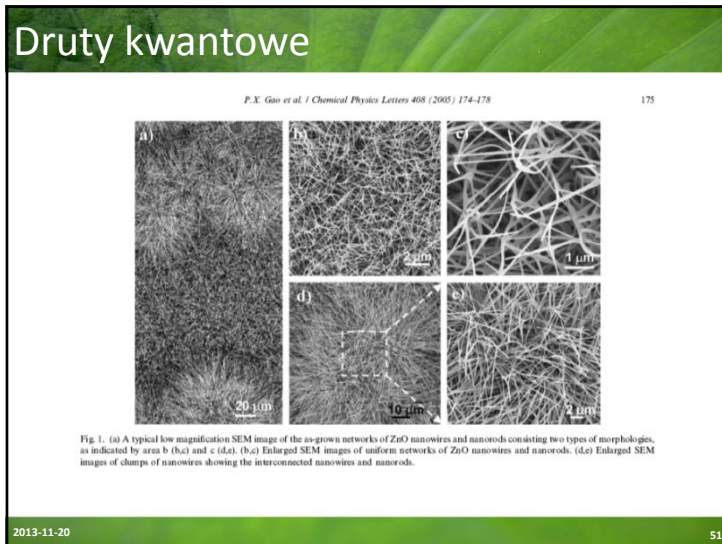
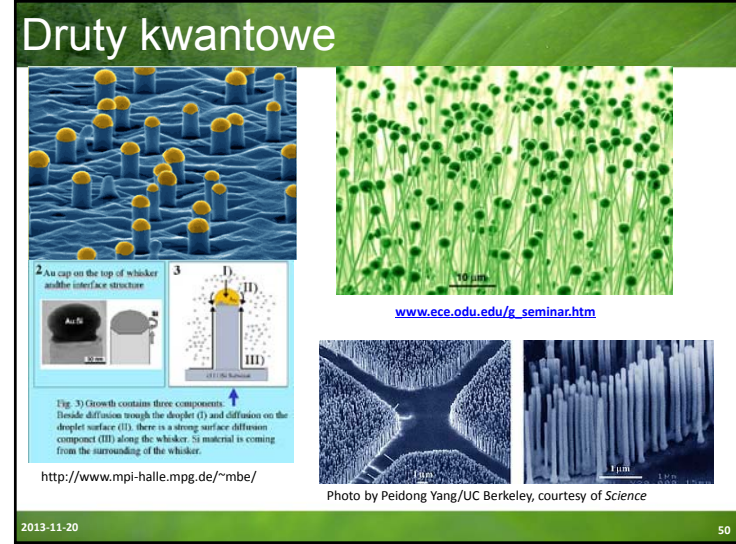
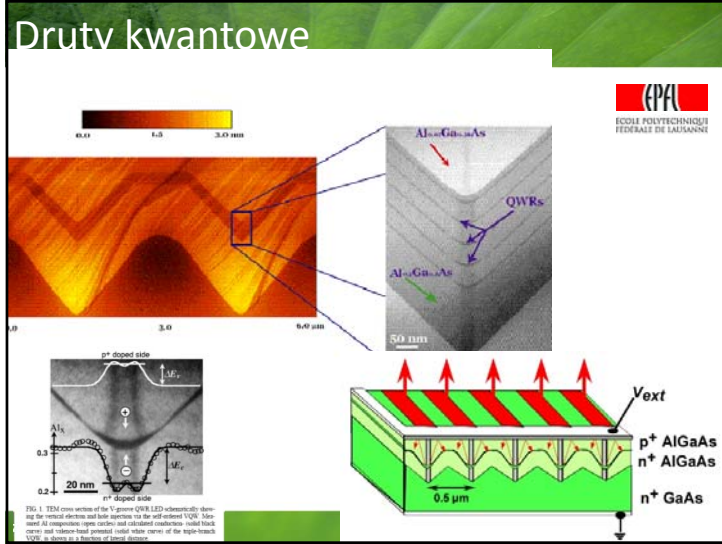
Druty kwantowe

Figure 9 Quantum wire fabrication based on nanoscale etching and re-growth

Figure 12 Selective growth of quantum wires on a pre-patterned V-groove substrate

Figure 11 Growth of quantum wires on a vicinal surface with multiatomic steps

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Struktury niskowymiarowe

Low-dimensional Semiconductor Systems

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Kropki kwantowe

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Dyskretna struktura elektronowa

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Quantum Dot

Hubert J. Krenner
Walter Schottky Institut and Physik Department E24, TU München

2013-11-20

Potencjał harmoniczny

EPITAXIAL LAYER
(e.g. InAs)

SUBSTRATE
(GaAs)

0.25µm x 0.25µm

Energy

Time

$\alpha_2 + \beta_{12} = \alpha_1$

Island formation

TEM

• Defect-free semiconductor “clusters” on a 2D quantum well wetting layer

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Potencjał harmoniczny 2D

GaAs InAs

AFM IMS-NRC

Digital Instruments NanoScope
Scan size 2,000 nm
Scan rate 1,000 Hz
Number of samples 512
Image Data
Data scale 100.0 nm

view angle
light angle
0 deg

X 0.500 nm/div
Z 100.000 nm/div

+0137.013

InGaAs QDs
50 nm

InGaAs QDs
20 nm

InGaAs QDs
5 nm

TEM J.Jasiński

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Synteza kropek kwantowych

Diagram illustrating the synthesis of quantum dots with different diameters (D) using precursors: C, H, O, Si, NH, OH, H, O. The resulting quantum dots are shown with diameters: D=390nm, D=313nm, D=454nm, and D=579nm.

<http://www.cnm.csic.es/cefe/Fab/synthesis.htm>

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Synteza kropek kwantowych

Photograph showing seven vials containing quantum dots of different sizes, demonstrating a color gradient from blue to red. The caption indicates CdSe/ZnS 1-10 nm.

<http://www.nanopicotheday.org/2003Pics/QDRainbow.htm>

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Energia

Illustrations showing a solar sail (left) and a CIGS solar cell structure (right).

<http://www.daystartech.com/lightfoil.cfm>

Cu(In,Ga)Se₂ (also called CIGS) compound semiconductor
solar electricity conversion efficiency of 12.8%

<http://www.tif.ethz.ch/HESC/HESC.html>

Labels for the solar cell structure: Encapsulation, ZnO, CdS, Cu(In,Ga)Se₂, Mo, Polyimide.

ETH
The Swiss Federal Institute of Technology Lausanne

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Nanotechnologia

CO?

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JAK?

- Top-down, czyli (nano)technologia
- Bottom-up, czyli samoorganizacja

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Top-down ↓



Vincent Laforet/The New York Times

2013-11-20

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<http://qt.tn.tudelft.nl/research/qdots/>

[Nano Tech Web](#)

[S. Kawata *et al.*, *Nature* **412**, 697 (2001)]

7μm

(3 hours to make)

$\lambda = 780\text{nm}$

resolution = **150nm**

2μm

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Jak To jest zrobione?

Focus Ion Beam



IEM-9320 Focused Ion Beam System



<http://www.norsam.com/>

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Jak To jest zrobione?

Focus Ion Beam



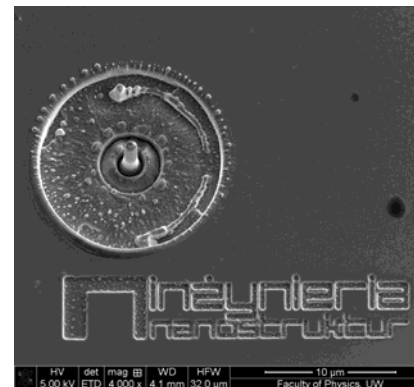
<http://www.fei.com/products/fib/vion/>

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Jak To jest zrobione?

Focus Ion Beam

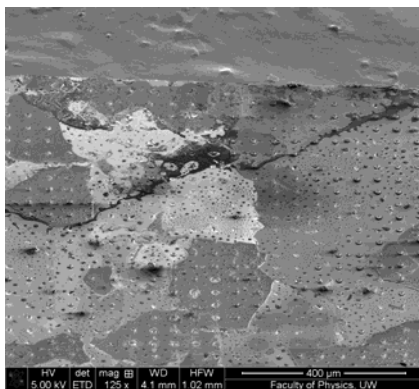


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Jak To jest zrobione?

Focus Ion Beam

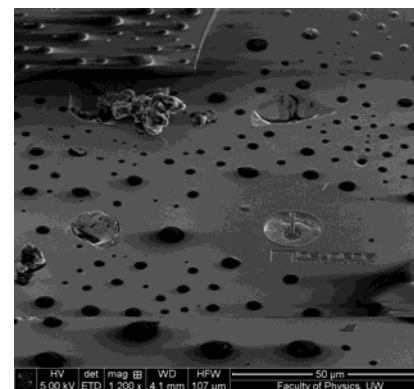


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Jak To jest zrobione?

Focus Ion Beam

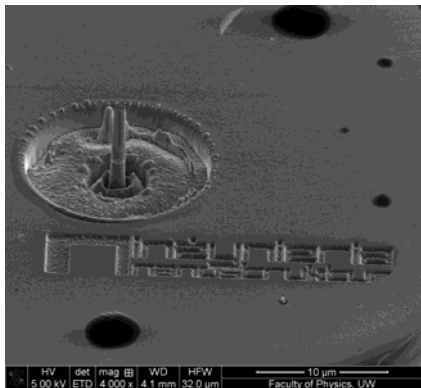


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Jak To jest zrobione?

Focus Ion Beam

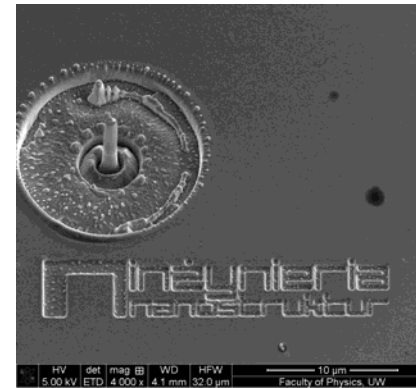


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Jak To jest zrobione?

Focus Ion Beam



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Jak To jest zrobione?

Focus Ion Beam

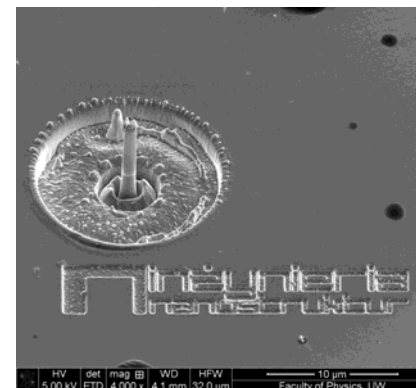


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Jak To jest zrobione?

Focus Ion Beam

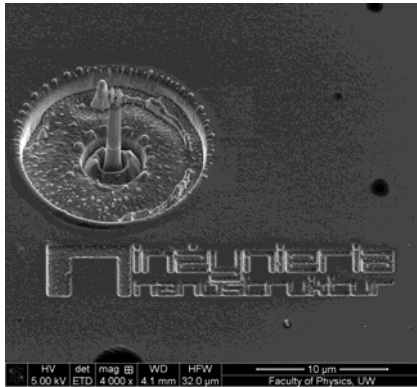


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Jak To jest zrobione?

Focus Ion Beam

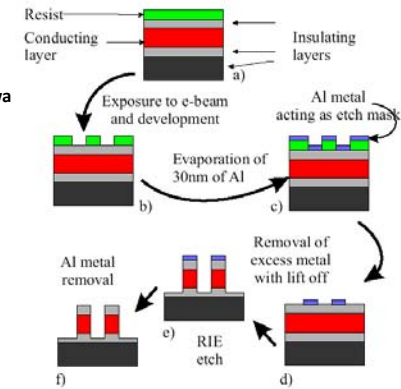


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Jak To jest zrobione?

1. Dominuje technologia krzemowa
2. Obecne układy ~ 10^9 - 10^{10} tranzystorów
3. Podłoża - 300mm, ~ 10^3 chipów
4. Fotolitografia, naświetlanie, trawienie etc
5. Typowo ~20 masek, 150 - 200 kroków procesów

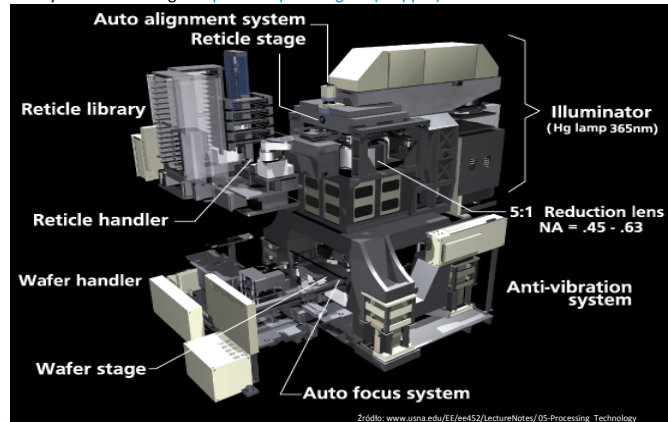


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Jak To jest zrobione?

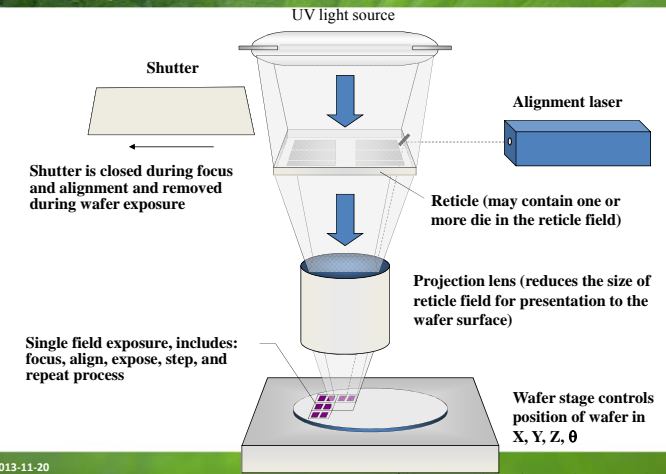
Maszyna do technologii Step-and-Repeat Aligner (Stepper)



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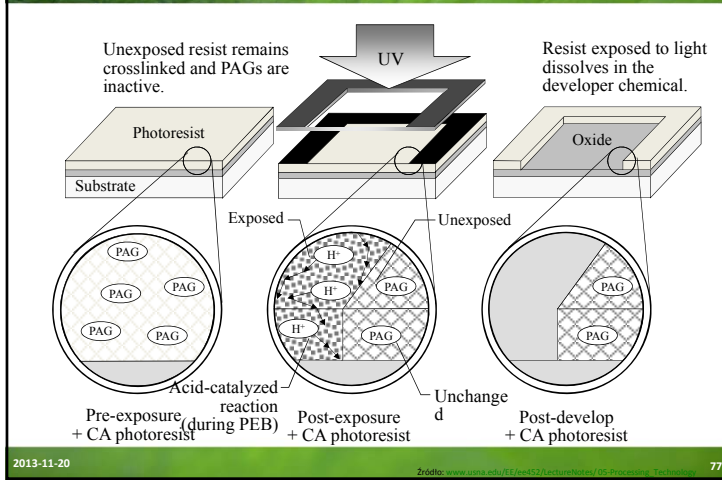
Jak To jest zrobione?



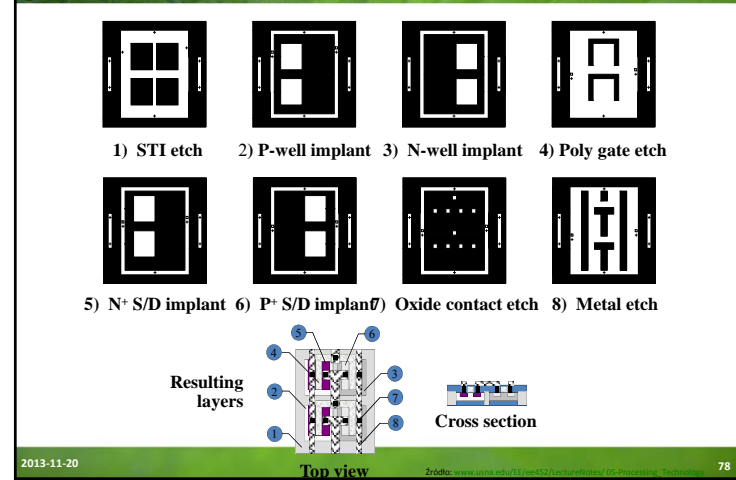
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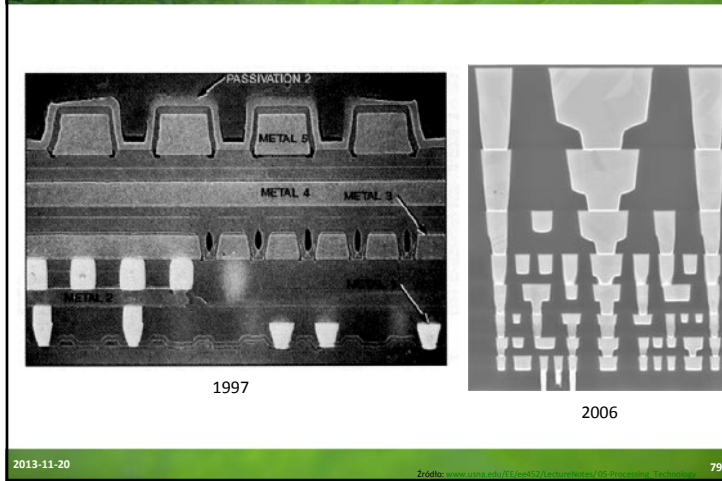
Jak To jest zrobione?



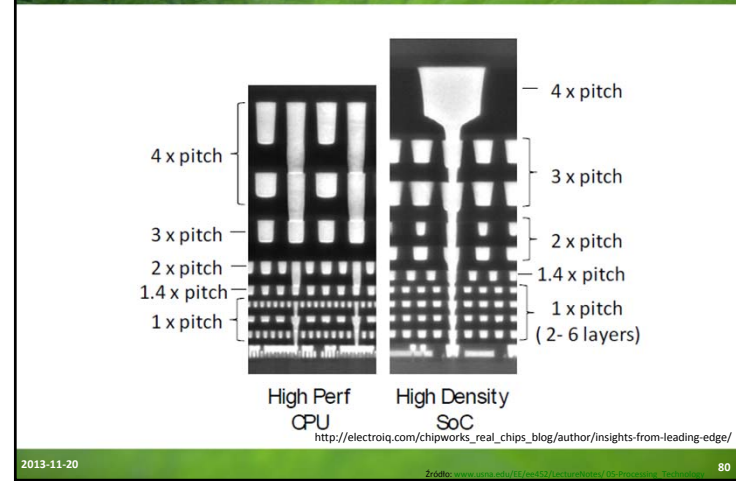
Jak To jest zrobione?



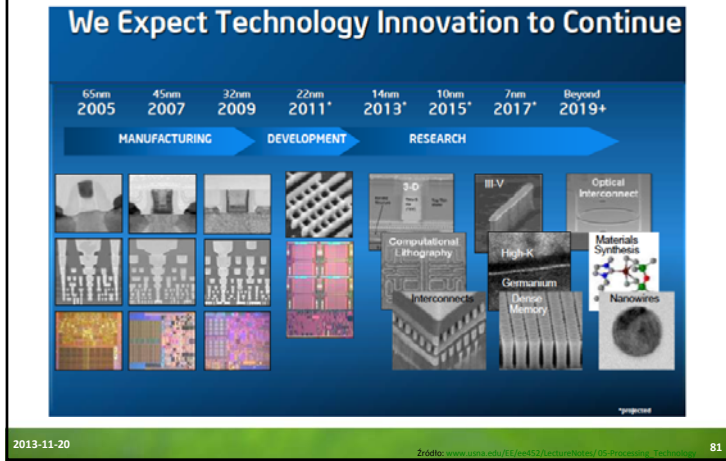
Jak To jest zrobione?



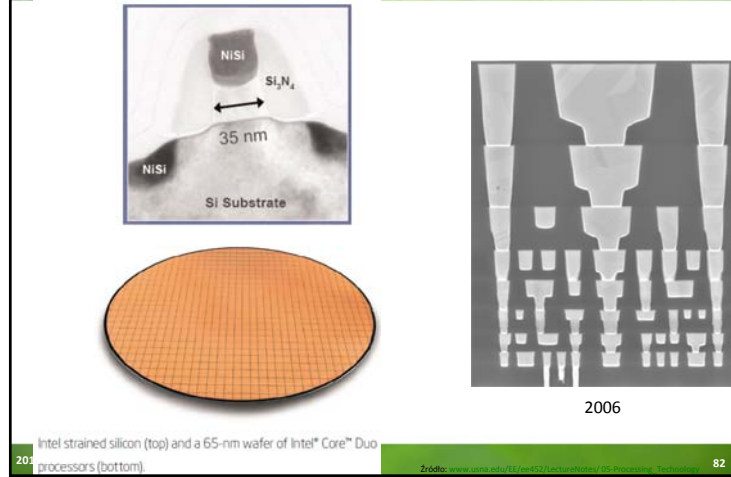
Jak To jest zrobione?



Jak To jest zrobione?



Jak To jest zrobione?

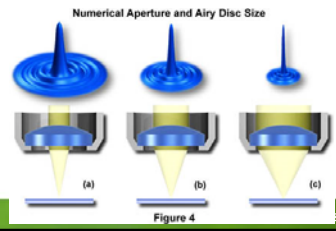
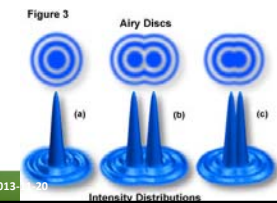
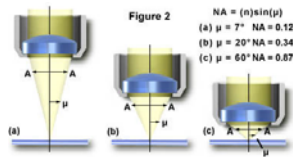


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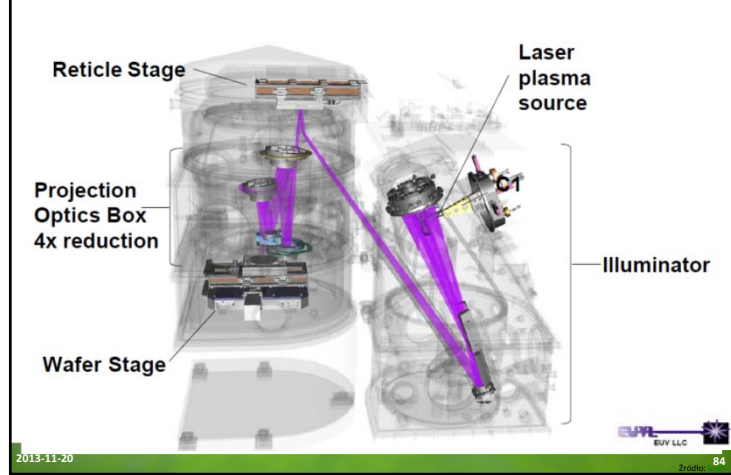
Zdolność rozdzielcza (kryterium Rayleigha)
 W – najmniejszy rozmiar dostępny w litografii, mikroskopii etc.

$$NA = n \sin \alpha = d / (2f)$$

$$W = \frac{k_1 \lambda}{NA}$$



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Litografia

Intel's Micro Exposure Tool (MET)



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Zdroj: 85

Litografia



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Zdroj: 86

Litografia

© MICRODESIGN RESOURCES JUNE 19, 2000 MICROPROCESSOR REPORT

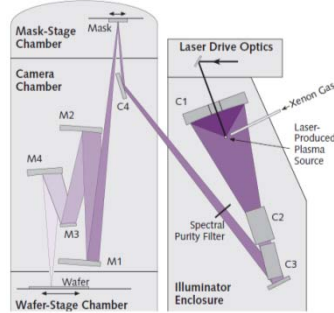


Figure 1. EUV light is generated from a 45eV plasma created when a 1,700W pulsed YAG solid-state laser illuminates a supersonic jet of xenon gas. The EUV light is collected and focused on a 4x reflective mask by a series of condenser mirrors (C1-C4). The mask image is projected onto the wafer by a 4x reduction camera (M1-M4) while the mask and wafer are simultaneously scanned. The entire operation takes place in high-vacuum environmental enclosures.



Figure 2. This engineering prototype of the engineering test stand (ETS) illuminator shows the LP light source and the C1 condenser assembly (top center). Small trapezoidally shaped doors protect the six C1-mirror petals when the ETS is not in operation. The entire condenser weldment, which also holds C2 and C3, is isolated from its environmental chamber to eliminate motion and vibration from the vacuum pumps. (Photo courtesy of Sandia National Lab)

Litografia

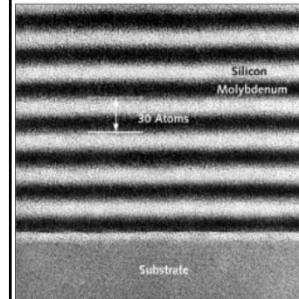


Figure 5. Each of the seven normal-incidence mirrors (including the mask) in the ETS is coated with 40 bilayers of molybdenum and silicon that are $\lambda/2$ (30 atoms) thick, creating a distributed Bragg reflector. Total reflectance at 13.5nm is 70%. (Source: Lawrence Livermore Lab)

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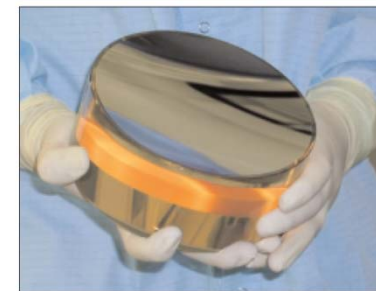


Photo by Keith Diefendorff

Figure 7. This photograph shows a polished and coated M4 mirror from the ETS camera. For people who appreciate ultrahigh precision, the mirror is a thing of beauty.

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Litografia imersyjna

http://www.microscopy.fsu.edu/

Zdolność rozdzielcza (kryterium Rayleigha)
 $W = \text{najmniejszy rozmiar dostępny w litografii, mikroskopii etc.}$

Figure 2

$NA = (n) \sin(\mu)$
 (a) $\mu = 7^\circ$ NA = 0.12
 (b) $\mu = 20^\circ$ NA = 0.34
 (c) $\mu = 60^\circ$ NA = 0.87

$$W = \frac{k_1 \lambda}{NA}$$

Figure 3

Airy Discs

Figure 4

Numerical Aperture and Airy Disc Size

2013-11-20 Intensity Distributions 89

Litografia

Intel, 2003

Litografia	90nm	65nm	45nm	32nm
Produkcja	2003 2005	2007	2009	

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Litografia

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Litografia

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Litografia

Mask Making Tutorial

Barry Lieberman, Ph.D.
Engineering Manager
Intel Mask Operation

What we ask for ← What we get →

“small” lens “medium” lens “large” lens

OPC – Optical Proximity Corrections

Example of OPC

Want this Ask for this On the mask Get this On the wafer

intel

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Litografia

Sub-resolution Optical Proximity Correction

Drawn structure Add OPC features Mask structure Printed on wafer

Phase shift masks enable patterning 35 nm lines

Drawn structure Add phase regions Mask structure Printed on wafer

0° 180° 0° 0° 180°

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OPC – Optical Proximity Corrections

RET “embellishments” must be fully resolved on the mask

Image on the wafer
NOT OUT of FOCUS!

820 nm 130 nm

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Litografia

OPC – Optical Proximity Corrections

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Some Mask-Making Metrics and Comparisons

- Pixels:**
 - On a 90 nm technology node mask: 1,000,000,000,000
 - In a high quality digital photo: 4,000,000
- Defects:**
 - Size that must be found and repaired: 0.1 micron
 - Number of such defects allowed: 0
 - Size ratio: defect to the mask area: size of a basketball area of California
- Data**
 - Typical number of mask layers for 90 nm generation logic product: 22-25
 - Total file size needed to specify all these layers: 200 GB
 - Time to transmit (design site to mask shop) using T1 line (1.4 MB/sec): ~1.5 days
 - Time using T3 line (40 MB/sec): ~1.5 hours
- Cost**
 - Cost to lease a T3 line: \$70K/month
 - Capital cost to build a 90 nm node capable mask shop (capacity of 200 sets/year @50-70% yield): \$200-250M
 - Yearly cost to operate such a shop: \$60-100M
 - Cost to make a 90 nm node mask set (depreciation, labor, etc): ~\$800K-1.3M

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Litografia imersyjna



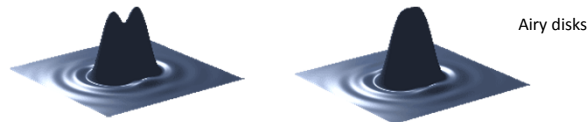
$$W = \frac{k_1 \lambda}{NA}$$

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Litografia imersyjna

Zdolność rozdzielcza (kryterium Rayleigha)
 W – najmniejszy rozmiar dostępny w litografii, mikroskopii etc.



The third element in the Rayleigh equation is k_1 . k_1 is a complex factor of several variables in the photolithography process such as the quality of the photoresist and the use of resolution enhancement techniques such as phase shift masks, off-axis illumination and optical proximity correction. While exposure wavelengths have been falling and NA rising, k_1 has been falling as well. See figure 2. The practical lower limit for k_1 is thought to be ~0.25.

$$W = \frac{k_1 \lambda}{NA}$$

$$W = \frac{0.25 \times 193}{0.93} = 52nm$$

$$W = \frac{k_1 \lambda}{n \sin \alpha} = \frac{0.25 \times 193}{1.47 \times 0.93} = 35nm$$

$$NA = n \sin \alpha = d / (2f)$$

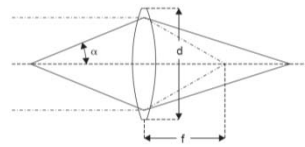


Figure 3. Numerical aperture.

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Litografia imersyjna

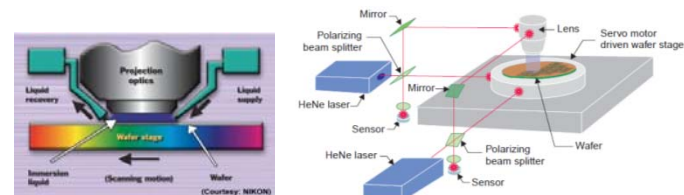


Figure 4. Stepping exposure system stage control

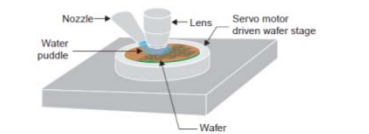
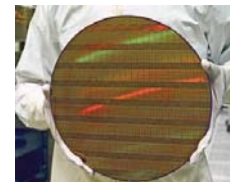


Figure 5. Immersion lithography. Stage control omitted for clarity.

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http://www.smalltimes.com/articles/stm_print_screen.cfm?ARTICLE_ID=260007

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Litografia imersyjna

Schematic showing factors of concern at resist/overcoat/fluid interfaces

http://www.almaden.ibm.com/st/chemistry/lithography/immersion/resist_development/

2013-11-20 <http://www.microelectronics.be/wwwinter/mediacenter/en/SR2005/html/142296.htm>

Litografia imersyjna

Beyond3D TSMC: 45nm ready in September

News: Reviews, Articles, Interviews, PR, JPR, 3D Resources, Forums

Latest Reviews: AMD R6xx: Image Quality Analysis w/ AA focus, Sapphire Ultimate Radeon HD 2400 XT - Early Peak, NVIDIA Quadro FX 5600, Galaxy GeForce 8800 GE, AMD RV530 and RV530 Introduction

Latest News: Bungie Studios to gain independence, New P53 model to hit Europe for 399 EUR, Enemy Territory: Quake Wars

TSMC: 45nm ready in September
Tuesday 10th April 2007, 07:45:10 AM, written by Arnan

TSMC has announced that their low-power 45nm process will be entering production in September, with general purpose and high performance variants following sooner rather than later. Traditionally, handheld chipsets will be the first to use a new process as they have much lower yield requirements. PPGAs, as per their highly symmetric nature and their redundancy mechanisms, are also among the first adopters of a given process node. Desktop and laptop GPUs, on the other hand, tend to lag behind by 18 to 24 months.

For example, TSMC 65nm production started on the low-power

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Litografia imersyjna

AMD and IBM Detail Early Results Using Immersion and Ultra Low-K in 45nm Chips

At the International Electron Device Meeting today, IBM and AMD presented papers describing the use of immersion lithography, ultra-low-K interconnect dielectrics, and multiple enhanced transfer strain techniques for application to the 45nm microprocessor process generation. AMD and IBM expect the first 45nm products using immersion lithography and ultra-low-K interconnect dielectrics to be available in mid-2008.

As the first microprocessor manufacturers to announce the use of immersion lithography and ultra-low-K interconnect dielectrics for the 45nm technology generation, AMD and IBM continue to blaze a trail of innovation in microprocessor process technology," said Nick Kogler, vice president of logic technology development at AMD. "Immersion lithography will allow us to deliver enhanced microprocessor design definition and manufacturing consistency, further increasing our ability to deliver industry-leading, highly sophisticated products to our customers. Ultra-low-K interconnect dielectrics will further extend our industry-leading microprocessor performance-per-watt ratio for the benefit of all of our customers. This announcement is another proof of IBM and AMD's successful research and development collaboration.

Current process technology uses conventional lithography, which has

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Inne

IBM Extends Moore's Law to the Third Dimension

An IBM scientist holds a thinned wafer of silicon computer circuits, which is ready for bonding to another circuit wafer, where IBM's advanced "through-silicon via" process will connect the wafers together by etching thousands of holes through each layer and filling them with metal to create 3-D integrated stacked chips. The IBM breakthrough can shorten wire lengths inside chips up to 1000 times and allow for hundreds more pathways for data to flow among different functions on a chip. This technique will extend Moore's Law beyond its expected limits, paving the way for a new breed of smaller, faster and lower power chips. Credit: IBM

IBM today announced a breakthrough chip stacking technology in a manufacturing environment that paves the way for three-dimensional chips that will extend Moore's Law beyond its expected limits. The technology - called "through-silicon vias" - allows different chip components to be packaged much closer together for faster, smaller, and lower-power systems.

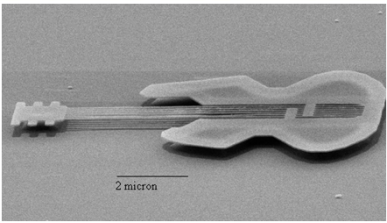
Semiconductor Process Tools - 24/7 Support, Restos, Upgrades Fully Restored Semtool, OEM Parts

Ultra uniform SOI wafer - MEMS Engineering & Material provides ultra uniform SOI wafer

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Litografia 3D

Lasery ekscymerowe

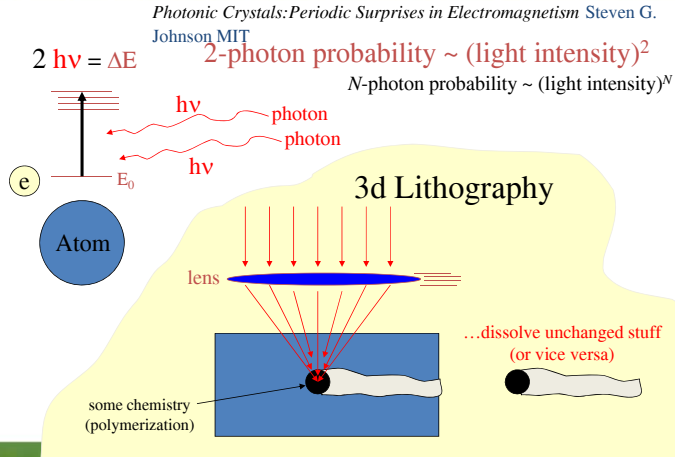


Electron-microscope image of the world's smallest guitar, based roughly on the design for the Fender Stratocaster, a popular electric guitar. Its length is 10 millionths of a meter—approximately the size of a red blood cell and about 1/20th the width of a single human hair. Its strings have a width of about 50 billionths of a meter (the size of approximately 100 atoms). Plucking the tiny strings would produce a high-pitched sound at the inaudible frequency of approximately 10 megahertz. Made by Cornell researchers with a single silicon crystal, this tiny guitar is a playful example of nanotechnology, in which scientists are building machines and structures on the scale of billionths of a meter to perform useful technological functions and study processes at the submicroscopic level. (Image courtesy Dustin W. Carr and Harold G. Craighead, Cornell.)

Litografia 3D

Photonic Crystals: Periodic Surprises in Electromagnetism Steven G. Johnson MIT

$2 h\nu = \Delta E$ 2-photon probability $\sim (\text{light intensity})^2$
 N-photon probability $\sim (\text{light intensity})^N$

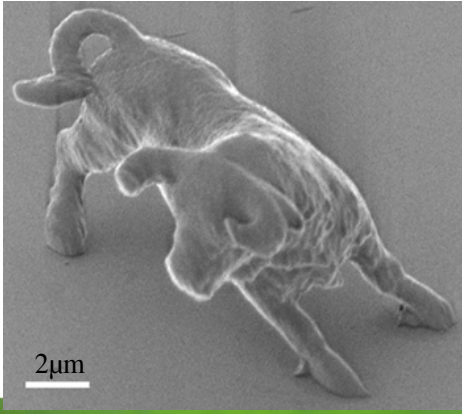


3d Lithography

some chemistry (polymerization) ...dissolve unchanged stuff (or vice versa)

Litografia 3D

[S. Kawata *et al.*, *Nature* **412**, 697 (2001)]

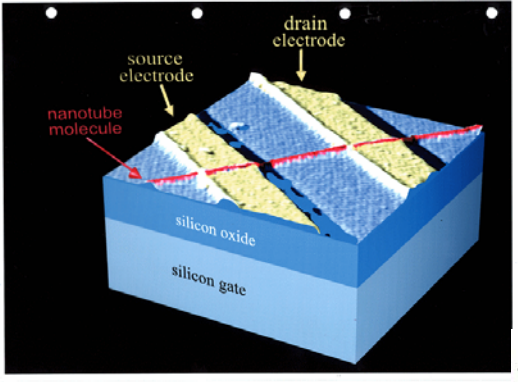


$\lambda = 780\text{nm}$
 resolution = 150nm
 7 μm
 (3 hours to make)

2 μm

Jak To jest zrobione?

Nanotubes as molecular quantum wires



source electrode drain electrode
 nanotube molecule
 silicon oxide
 silicon gate

Cees Dekker
 TU Delft DIMES

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Nanotechnologia

CO?

- Studnie, druty, kropki

JAK?

- Top-down, czyli (nano)technologia
- Bottom-up, czyli samoorganizacja

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Bottom-up ↑

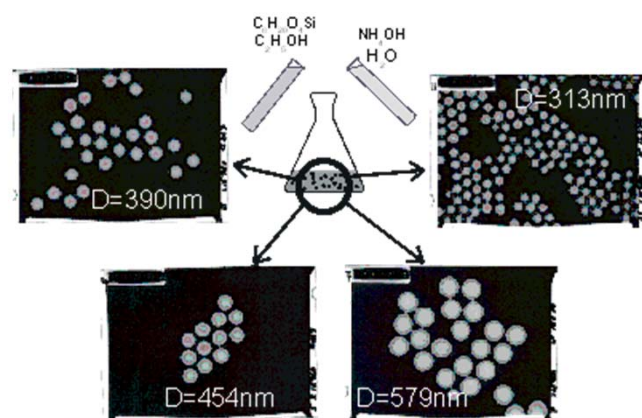


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Synteza kropek kwantowych



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Synteza kropek kwantowych



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