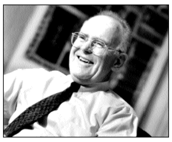
Powtórka:

Koniec technologii krzemowej? Prawo Moora i jego konsekwencje.

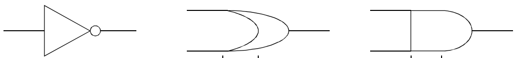
a. Trochę historii
b. Jak to działa
   i. Trochę logiki
   ii. Od bramki do bramki
   iii. Jak działa tranzystor
c. Prawo Moora
   i. Nanotechnologia
   ii. Domieszki – koncentracja i statystyka
   iii. Tunelowanie
   iv. Chłodzenie



Amara's law is a maxim stating:
We tend to overestimate the effect of a technology in the short run and underestimate the effect in the long run.

Uniwersytet Warszawski

Jak to działa? Trochę logiki



NOT	
0	1
1	0

OR	0	1
0	0	1
1	1	1

AND	0	1
0	0	0
1	0	1

XOR	0	1
0	0	1
1	1	0

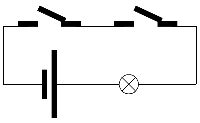
NOR	0	1
0	1	0
1	0	0

NAND	0	1
0	1	1
1	1	0

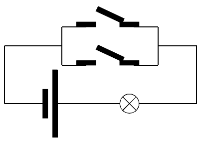
XNOR	0	1
0	1	0
1	0	1

Od bramki do bramki.

AND



OR

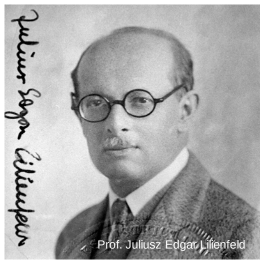


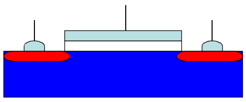
AND	0	1
0	0	0
1	0	1

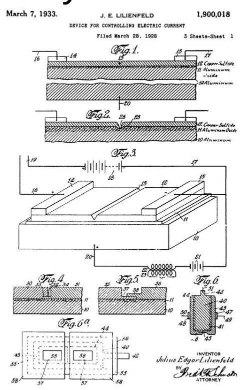
OR	0	1
0	0	1
1	1	1

Jak działa tranzystor?

18.04.1881, (Lemberg)- 8.08.1963, (Charlotte Amalie, U.S.A.)

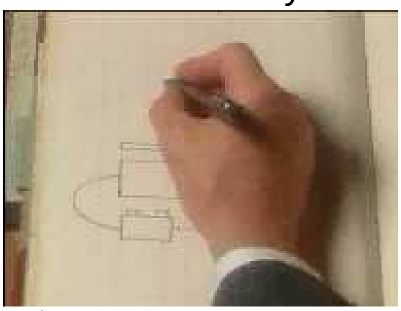


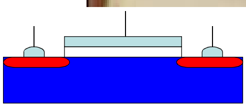




http://chem.ch.huji.ac.il/history/lilienfeld.htm

Jak działa tranzystor?





Prof. Juliusz Edgar Lilienfeld
1925 tranzystor polowy Cu_2S (Lipsk)

http://www.pbs.org/transistor/science/events/pointcrans.html

Nanotechnologia

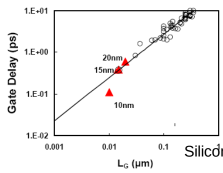


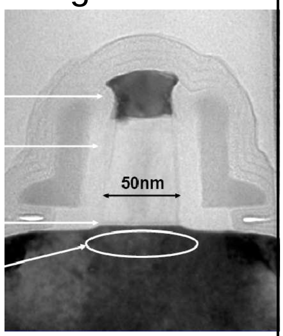
Figure 3: Gate delay vs. transistor physical gate length L_G.

Silicide layer

Silicon gate elctrode

1.2 nm SiO_2 gate oxide

Strained Silicon



50 nm generation transistor (Intel 2003)

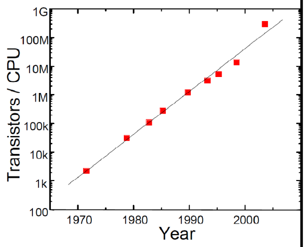
Intel 2Q 2003:
Oxide thickness: ~ 3 nm
Channel length: ~ 90 nm
Gate position: ~ 6 nm (!)
Characteristic time: ~ 1.6 ps
Subthreshold leakage: 0.01 mA/micron
Parasitic *RSD* contribution: < 16%
Energy per switching: 0.35 fJ
Static power dissipation: 5.6 nW

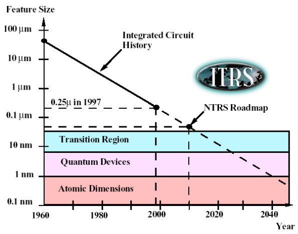
Źródło: Intel

TRENDY: Pierwsze Prawo Moore'a

Ilość komponentów (tranzystory, połączenia, izolacje itd.) w IC podwaja się co około 18 miesięcy.

Rozmiar liniowy komponentów również zmniejsza się wykładniczo w czasie.





Te trendy nie mogą być kontynuowane w nieskończoność.

- Co zastąpi technologię Si?
- Z czego będzie wynikała ta zmiana technologii?

EKONOMIA

Źródło: Intel

NO EXPONENTIAL IS FOREVER...

BUT WE CAN DELAY „FOREVER”

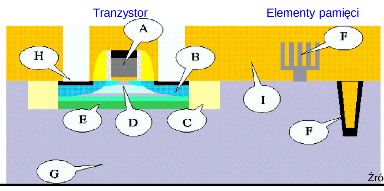
Gordon Moore, 2003

International Technology Roadmap for Semicond.

SEMATECH Accelerating the next technology revolution.

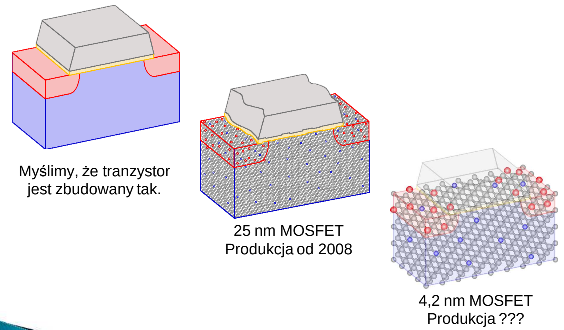
SEMATECH: międzynarodowe konsorcjum producentów półprzewodników – określa cele, opłaca badania nad rozwiązaniem problemów dotyczących „wszystkich”, w jego skład wchodzą: AMD, Agere Systems, Hewlett-Packard, Hynix, Infineon Technologies, IBM, Intel, Motorola, Philips, STMicroelectronics, Texas Instruments

Stara się zdefiniować "wyzwania technologiczne", określić dalsze cele i przewidzieć ich specyfikację, koszt, wydajność, czas wdrożenia itp.



Źródło: Intel, Sematech

Granice miniaturyzacji?

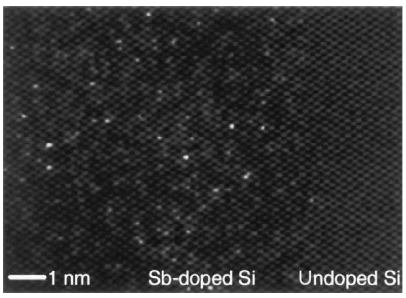


Asen Asenov, Glasgow
David Williams *Hitachi-Cambridge*

IEEE Trans Electron Dev 50(9), 1837 (2003)

PROBLEM: Statystyka domieszek

Voyles, P. M. *et al.* *Nature* **416**, 826-829 (2002)

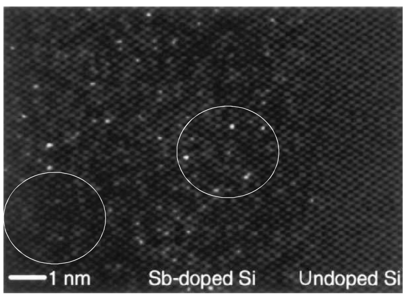


10^{22} atomów Si
10^{17} domieszek
Rozmiar tranzystora 50 nm
Średnia ilość domieszek 12.5

State-of-the-art TEM image of ultrathinned (5 nm) sample.

PROBLEM: Statystyka domieszek

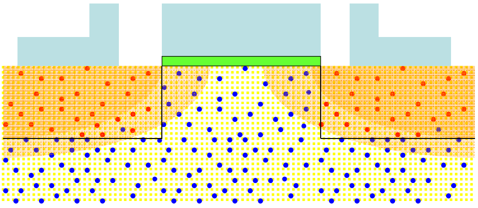
Voyles, P. M. *et al.* *Nature* **416**, 826-829 (2002)



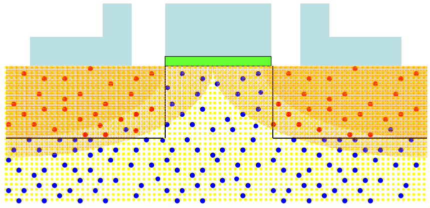
10^{22} atomów Si
10^{17} domieszek
Rozmiar tranzystora 50 nm
Średnia ilość domieszek 12.5

State-of-the-art TEM image of ultrathinned (5 nm) sample.

PROBLEM: Tunelowanie

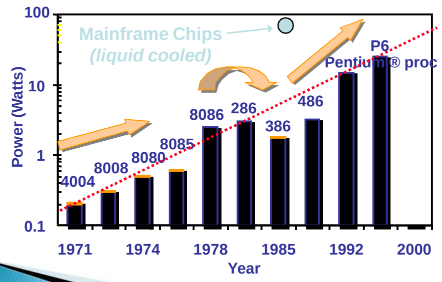


PROBLEM: Tunelowanie



PROBLEM: Chłodzenie

Z roku na rok układy wymagają większej mocy do wykonywania operacji logicznych.

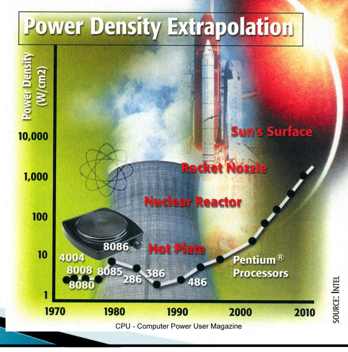


PROBLEM: Chłodzenie

Gęstość mocy rośnie dramatycznie.

10^7 tranzystorów pracujących z częstością 1.5 GHz zużywa 130 W. Zakładając, że na tej samej powierzchni za jakiś czas będzie pracować 10^8 tranzystorów z częstością 10 GHz otrzymamy gęstość mocy na poziomie 10 kW/cm^2 (porównywalną gęstość mocy ma silnik rakietowy!)

Film



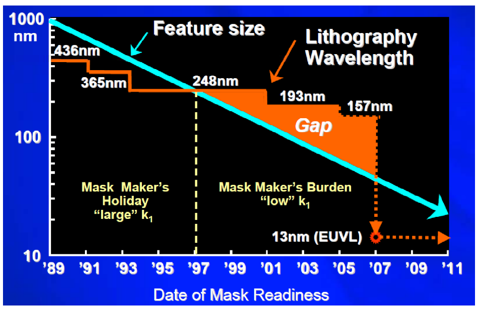
PROBLEM: Podłoża

Krzem 2003,
- wafer 30 mm:
- Wymagane jest nie więcej niż 120 cząstek <100 nm na wafer
- Dokładność polerowania 130 nm

Krzem 2007,
- wafer 30 mm:
- Wymagane jest nie więcej niż 77 cząstek <100 nm na wafer (jak to zmierzyć?)
- Dokładność polerowania 65 nm

Krzem 2016,
- wafer 450 mm:
- Wymagane jest nie więcej niż 77 cząstek <100 nm na wafer (jak to zmierzyć?)
- Dokładność polerowania 22 nm (jak to zmierzyć?)

PROBLEM: Litografia



PROBLEM: Litografia

Litografia 2003,
- Długość fali światła 248 nm
- Kanał FET 90 nm:
- Wymagane jest nie więcej niż 2000/m2 <100 nm
- Fluktuacje granic rezystu 7 nm

Litografia 2007,
- Długość fali światła 193 nm (?) 153 nm (?) X-ray (?)
- Kanał FET 35 nm:
- Wymagane jest nie więcej niż 1500/m2 <100 nm
- Fluktuacje granic rezystu 3 nm

Prawdopodobnie koniec epoki polimerowych rezystów (cząstki polimerów są zbyt duże!)

Litografia 2016,
- Długość fali światła X-ray (?)
- Kanał FET 9 nm:
- Wymagane jest nie więcej niż 500/m2 <100 nm
- Fluktuacje granic rezystu 1 nm

week09

PROBLEM: itd...

itd...

itd...

itd...

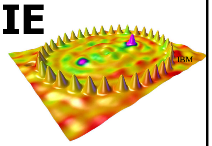
NOWE TECHNOLOGIE

- Przeprojektowanie CMOS (np. wertykalne, FIN, MOSFET z podwójną bramką)
- Urządzenia alternatywne (np. na pojedynczych elektronach)
- Urządzenia hybrydowe (np. FET z nanorurek)
- Nowe architektury (np. samonaprawiające się, defect-tolerance, automaty komórkowe)
- Zupełnie nowe architektury (np. komputery molekularne, komputery kwantowe)

ITRS

NOWE TECHNOLOGIE

Jacek.Szczytko@fuw.edu.pl



Dialog z przyrodą musi być prowadzony w języku matematyki, w przeciwnym razie przyroda nie odpowiada na nasze pytania.
Michał Heller

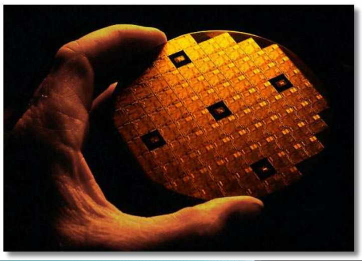
Koniec technologii krzemowej? Prawo Moora i jego konsekwencje (czyli o postępie technologicznym);
Nanotechnologia I (czyli nano jest trendy)
Kwanty, stany, pasma (czyli mechanika kwantowa dla początkujących);
Nanotechnologia II, III, IV (studnie, druty, kropki; nanorurki i nanomaszyny);
Spintronika stosowana; **Dlaczego elektrony kręcą?** (czyli o spinie);
Kwantowa kryptografia i teleportacja I i II (czyli o splątaniu kwantowym oraz kodach i kluczach);
Komputery kwantowe I i II (czyli o przyszłych informatykach oraz o przyszłych komputerach)
Badania i postęp (czyli o finansowaniu badań);
W smutnym kolorze blue (czyli o niebieskim laserze i białych diodach);
Optoelektronika (czyli o manipulowaniu światłem);
Nieliniowo, adaptacyjnie i femtosekundowo, czyli ekstremalnie w optyce;
Czy komputer może myśleć? Prezentacja prac studentów

Uwaga: Wykład może być zaliczony do godzin pozakierunkowych: przedmioty ogólnouniwersyteckie Wydziału Fizyki kod: **1100-NT-OG**

Top-down

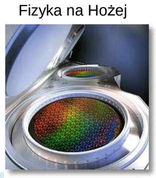
Vincent Laforet/The New York Times

Top-down, czyli małe jest piękne!



Prescot, Intel

Nanotechnologia
Litografia
Udoskonalenia
Galeria
Fizyka na Hożej



Uniwersytet Warszawski

Metoda Czochralskiego


Prof.Jan Czochralski 1885 - 1953,

Urodzony w 1885 roku jako ósmy syn ubogiego stolarza.
Nie jest pewne czy zdał maturę.
Nie stać go było na opłacenie studiów.
Odkrywca metody wzrostu kryształów - *"metody Czochralskiego"*.
Uznawany za *"praojca elektroniki"*
Polski uczony **najczęściej wymieniany w literaturze światowej**.
W Polsce prawie nieznany...

Metoda Czochralskiego

http://www.ptwk.org.pl/pol/patron.html

STANOWISKO SENACKIEJ KOMISJI HISTORII I TRADYCJI SZKOŁY PW W SPRAWIE UCHWAŁY SENATU Z DNIA 19 GRUDNIA 1945 R. DOTYCZĄCEJ PROF. DR. H.C. JANA CZOCHRALSKIEGO

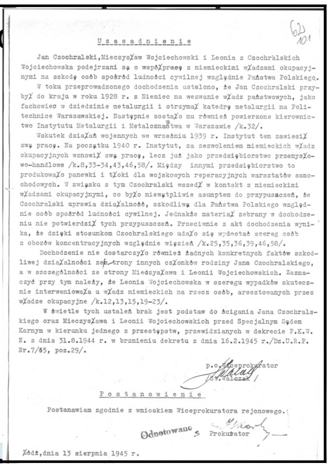
Jak wynika z zeznań świadków, w tym mgr. inż. Ludwika Szenderowskiego, b. kierownika warsztatu i odlewni w Zakładzie Badań Materiałów, a jednocześnie członka ruchu oporu, w r. 1942 na terenie ZBM rozpoczęła swą potajemną działalność komórka organizacyjna AK w zakresie produkcji odlewów żeliwnych skorup do granatów, elementów drukarń polowych i części do pistoletów. Prof. Czochralski wiedział o tym i nie tylko tolerował, ale i ochraniał działalność konspiracyjną w swym zakładzie wobec władz niemieckich i gestapo.

Na korzyść prof. Czochralskiego należy również zaliczyć jego działalność poza ZBM. Wykorzystując swe rozległe znajomości, interweniował wielokrotnie i dość skutecznie u władz okupacyjnych w celu uwolnienia różnych osób z obozów niemieckich, więzień i obozów koncentracyjnych. Wśród osób uwolnionych można znaleźć m.in. nazwisko dr. Mariana Świderka, późniejszego profesora PW, wnuka Ludwika Solskiego.

Znamienna jest tu wypowiedź b. asystentki prof. Czochralskiego prof. dr Zofii Wendorff, że "nie zna ona przypadku, aby prof. Czochralski odmówił pomocy Polakom, którzy się do niego zwrócili".

Metoda Czochralskiego

http://www.ptwk.org.pl/pol/patron.html



U z a s a d n i e n i e

Jan Czochralski, Mieczysław Wojciechowski i Leonia z Czochralskich Wojciechowska podejrzani są o współpracę z niemieckimi władzami okupacyjnymi na szkodę osób spośród ludności cywilnej względnie Państwa Polskiego.

W toku przeprowadzonego dochodzenia ustalono, że Jan Czochralski przybył do kraju w roku 1928 r. z Niemiec na wezwanie władz państwowych, jako fachowiec w dziedzinie metalurgii i otrzymał katedrę metalurgii na Politechnice Warszawskiej. Następnie zostało mu również powierzone kierownictwo Instytutu Metalurgii i Metaloznawstwa w Warszawie /k.32/.

Wskutek działań wojennych we wrześniu 1939 r. Instytut ten zawiesił swą pracę. Na początku 1940 r. Instytut, za zezwoleniem niemieckich władz okupacyjnych wznowił swą pracę, lecz już jako przedsiębiorstwo przemysłowo-handlowe /k.8,33-34,43,46,58/. Między innymi przedsiębiorstwo to produkowało panewki i tłoki dla wojskowych reperacyjnych warsztatów samochodowych. W związku z tym Czochralski wszedł w kontakt z niemieckimi władzami okupacyjnymi, co było niewątpliwie asumptem do przypuszczeń, że Czochralski uprawia działalność, szkodliwą dla Państwa Polskiego względnie osób spośród ludności cywilnej. Jednakże materiał zebrany w dochodzeniu nie potwierdził tych przypuszczeń. Przeciwnie z akt dochodzenia wynika, że dzięki stosunkom Czochralskiego udało się wydostać szereg osób z obozów koncentracyjnych względnie więzień /k.25,35,36,39,46,58/.

Dochodzenie nie dostarczyło również żadnych konkretnych faktów szkodliwej działalności ze strony innych członków rodziny Jana Czochralskiego, a w szczególności ze strony Mieczysława i Leonii Wojciechowskich. Zaznaczyć przy tym należy, że Leonia Wojciechowska w szeregu wypadków skutecznie interweniowała u władz niemieckich na rzecz osób, aresztowanych przez władze okupacyjne /k.12,13,15,19-23/.

W świetle tych ustaleń brak jest podstaw do ścigania Jana Czochralskiego oraz Mieczysława i Leonii Wojciechowskich przed Specjalnym Sądem Karnym w kierunku jednego z przestępstw, przewidzianych w dekrecie P.K.W.N. z dnia 31.8.1944 r. w brzmieniu dekretu z dnia 16.2.1945 r./Dz.U.R.P. Nr.7/45, poz.29/.

p.o. Wiceprokurator
/St. Walczak/

P o s t a n o w i e n i e

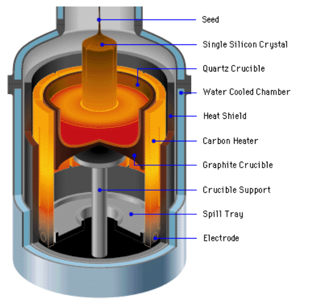
Postanawiam zgodnie z wnioskiem Wiceprokuratora rejonowego.

Odnotowano
Prokurator

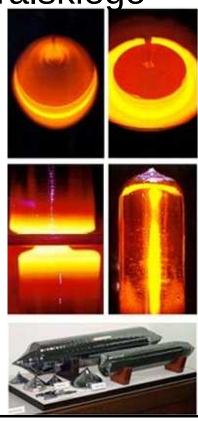
Łódź, dnia 13 sierpnia 1945 r.

Uzasadnienie Sądu i decyzja o zwolnieniu z zarzutów, Łódź , dnia 13.sierpnia 1945r

Metoda Czochralskiego



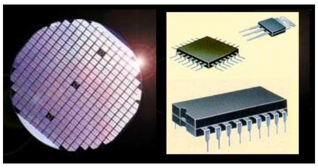
http://people.seas.harvard.edu/~jones/es154/lectures/lecture_2/materials/materials.html



http://www.sehmy.com/Product/abtWafers.htm

Metoda Czochralskiego

http://www.sehmy.com/Product/abtWafers.htm



Metoda Czochralskiego

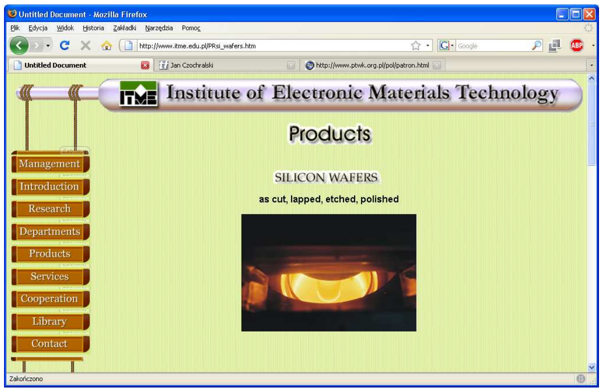
© "Smithsonian", Jan 2000, Vol 30, No. 10

http://www.tf.uni-kiel.de/matwis/amat/elmat_en/kap_6/backbone/r6_1_2.html

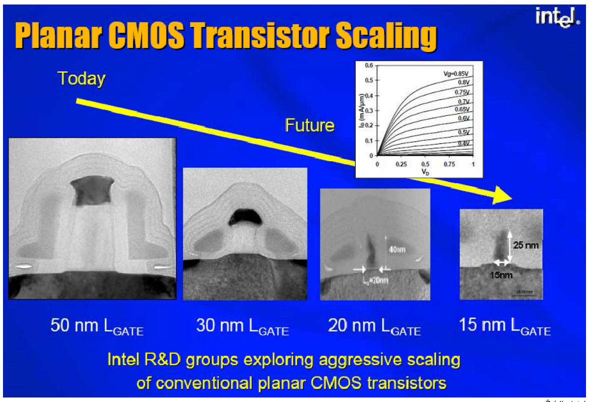
Czego/kogo brakuje w Polsce

Uniwersytet Warszawski

Metoda Czochralskiego

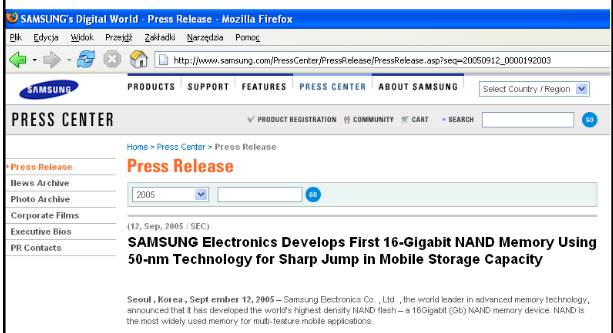


Nanotechnologia



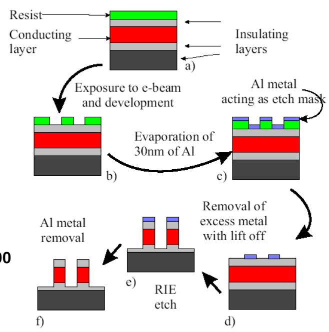
Źródło: Intel

Gdzie jest limit



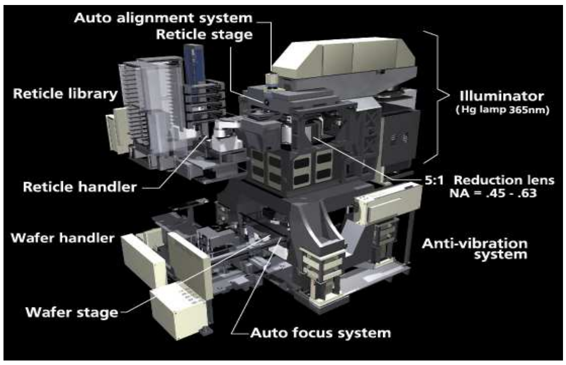
W jaki sposób produkowane są układy scalone?

1. **Dominuje technologia krzemowa**
2. **Obecne układy ~ 10^9 - 10^{10} tranzystorów**
3. **Podłoża - 300mm, ~ 10^3 chipów**
4. **Fotolitografia, naświetlanie, trawienie etc**
5. **Typowo ~20 masek, 150 - 200 kroków procesów**



Nanotechnologia

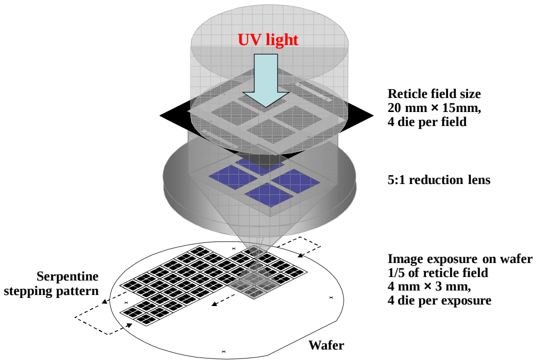
Maszyna do technologii Step-and-Repeat Aligner (Stepper)



Źródło: www.usna.edu/EE/ee452/LectureNotes/05-Processing_Technology

Litografia

Maszyna do technologii Step-and-Repeat Aligner (Stepper)



Źródło: www.usna.edu/EE/ee452/LectureNotes/05-Processing_Technology

Nanotechnologia

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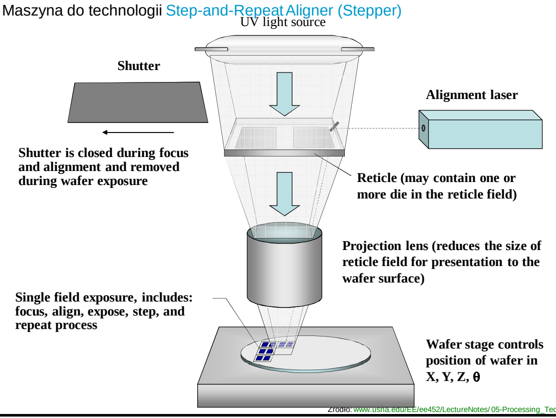
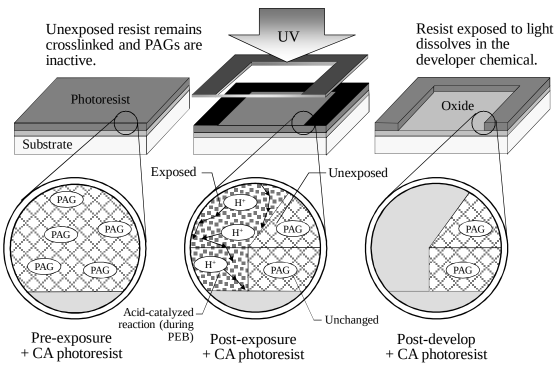


Źródło: www.usna.edu/EE/ee452/LectureNotes/05-Processing_Technology

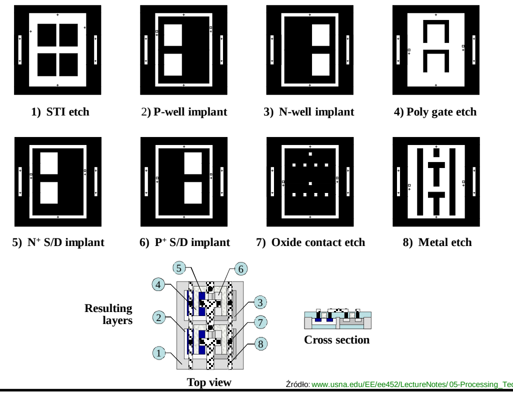
Nanotechnologia

Maszyna do technologii Step-and-Repeat Aligner (Stepper)



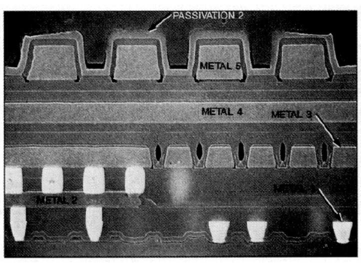
Źródło: www.usna.edu/EE/ee452/LectureNotes/05-Processing_Technology

Nanotechnologia

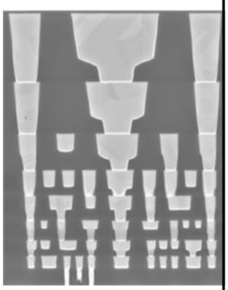


Źródło: www.usna.edu/EE/ee452/LectureNotes/05-Processing_Technology

Nanotechnologia



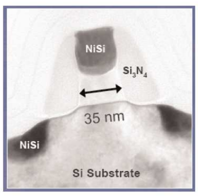
1997

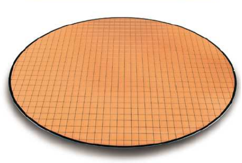


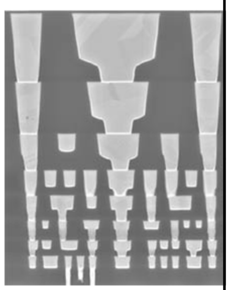
2006

Źródło: www.usna.edu/EE/ee452/LectureNotes/05-Processing_Technology

Nanotechnologia







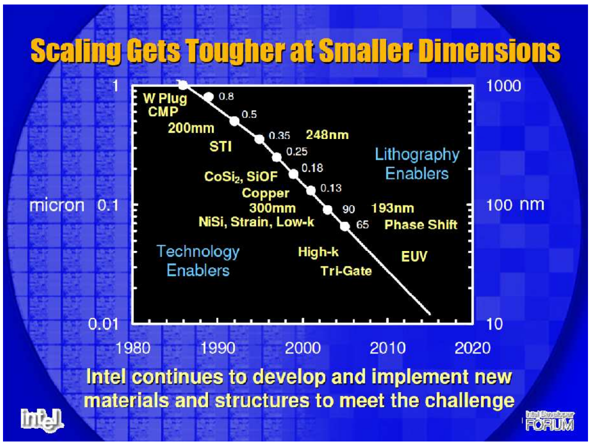
2006

Intel strained silicon (top) and a 65-nm wafer of Intel® Core™ Duo processors (bottom).

Źródło: www.usna.edu/EE/ee452/LectureNotes/05-Processing_Technology

Nanotechnologia

Film



http://www.microscopyu.com/

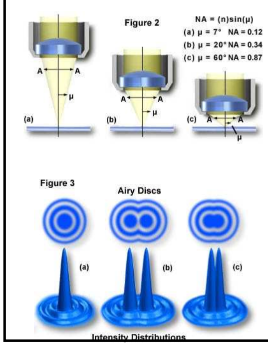
Litografia

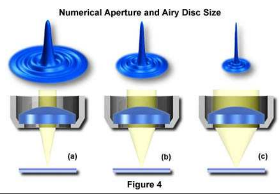
Zdolność rozdzielcza (kryterium Rayleigha)

W – najmniejszy rozmiar dostępny w litografi, mikroskopii etc.

$$NA = n \sin\alpha = d/(2f)$$

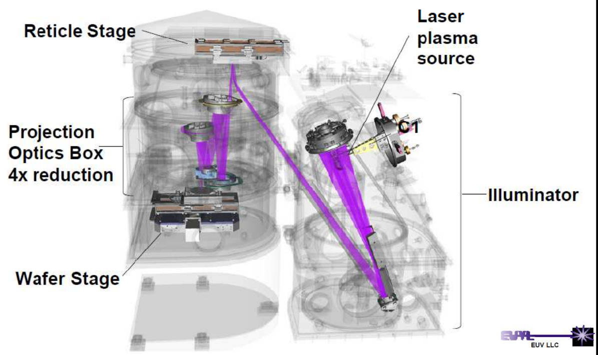
$$W = \frac{k\lambda}{NA}$$





Nanotechnologia

Maszyna do technologii Step-and-Repeat Aligner (Stepper)



Źródło: Intel

Nanotechnologia

Maszyna do technologii Step-and-Repeat Aligner (Stepper)

Źródło: Intel

Nanotechnologia

© MICRODESIGN RESOURCES JUNE 19, 2000 MICROPROCESSOR REPORT

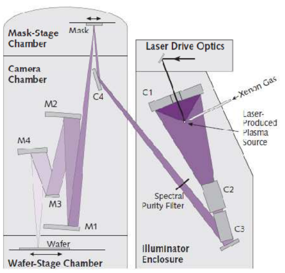


Figure 1. EUV light is generated from a 45eV plasma created when a 1,700W pulsed YAG solid-state laser illuminates a supersonic jet of xenon gas. The EUV light is collected and focused on a 4x reflective mask by a series of condenser mirrors (C1–C4). The mask image is projected onto the wafer by a 4x reduction camera (M1–M4) while the mask and wafer are simultaneously scanned. The entire operation takes place in high-vacuum environmental enclosures.

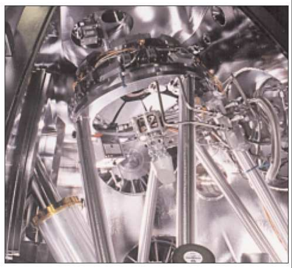


Figure 2. This engineering prototype of the engineering test stand (ETS) illuminator shows the LPP light source and the C1 condenser assembly (top center). Small trapezoidally shaped doors protect the six C1-mirror petals when the ETS is not in operation. The entire condenser weldment, which also holds C2 and C3, is isolated from its environmental chamber to eliminate motion and vibration from the vacuum pumps. (Photo courtesy of Sandia National Lab)

Nanotechnologia

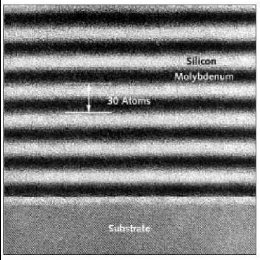


Figure 5. Each of the seven normal-incidence mirrors (including the mask) in the ETS is coated with 40 bilayers of molybdenum and silicon that are λ/2 (30 atoms) thick, creating a distributed Bragg reflector. Total reflectance at 13.5nm is 70%. (Source: Lawrence Livermore Lab)

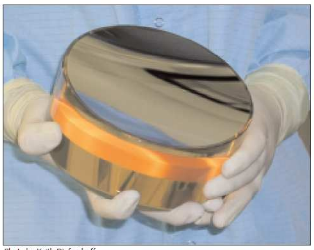
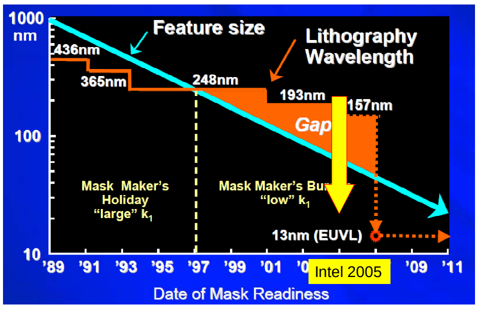


Photo by Keith Diefendorff

Figure 7. This photograph shows a polished and coated M4 mirror from the ETS camera. For people who appreciate ultrahigh precision, the mirror is a thing of beauty.

Nanotechnologia

Intel, 2003

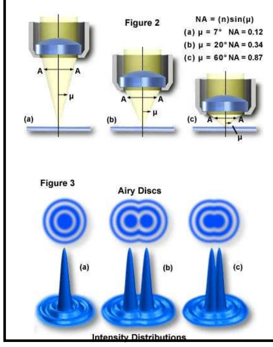


Litografia	90nm	65nm	45nm	32nm
Produkcja	2003	2005	2007	2009

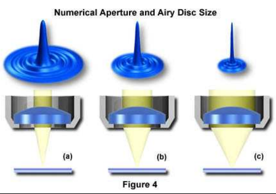
http://www.microscopy.fsu.edu/

Litografia Imersyjna

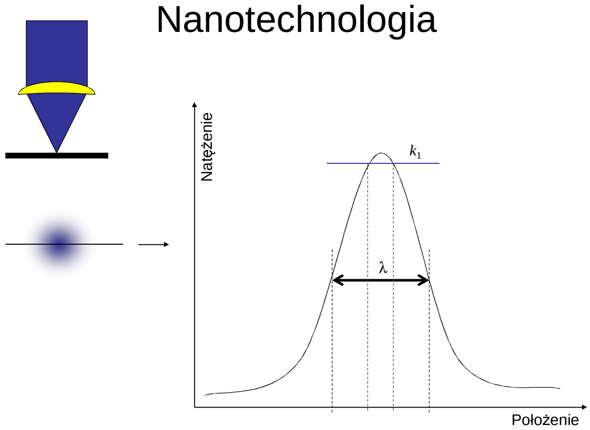
Zdolność rozdzielcza (kryterium Rayleigha)
W – najmniejszy rozmiar dostępny w litografi, mikroskopii etc.



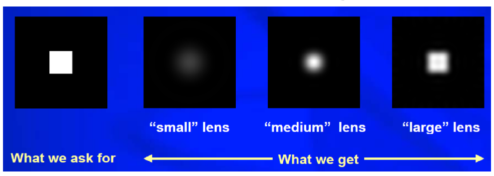
$$W = \frac{k_1 \lambda}{NA}$$



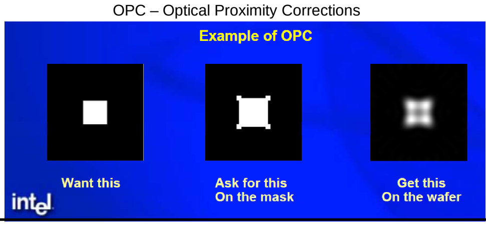
Nanotechnologia



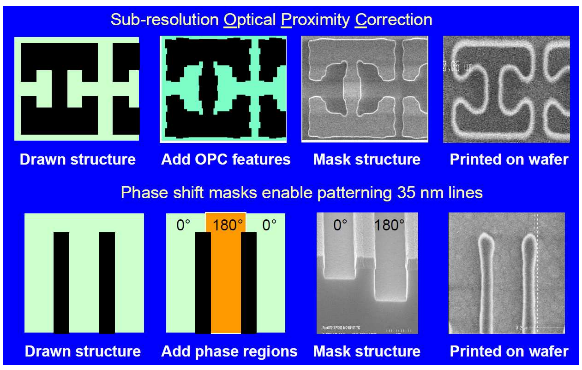
Nanotechnologia



OPC – Optical Proximity Corrections

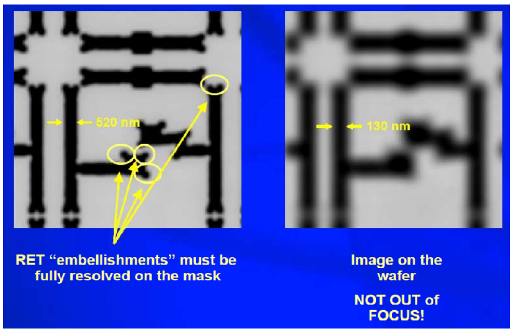


Nanotechnologia



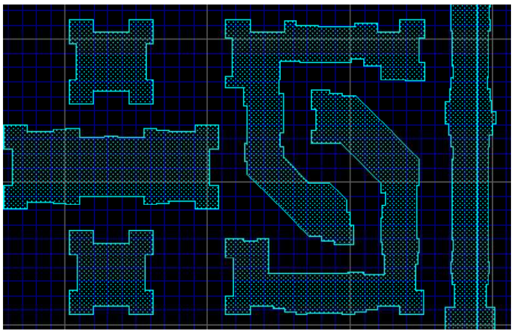
Nanotechnologia

OPC – Optical Proximity Corrections



Nanotechnologia

OPC – Optical Proximity Corrections



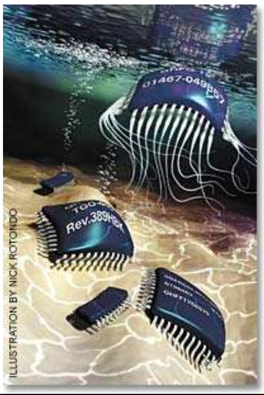
Nanotechnologia

Some Mask-Making Metrics and Comparisons

- **Pixels:**
  - On a 90 nm technology node mask: 1,000,000,000,000
  - In a high quality digital photo: 4,000,000
- **Defects:**
  - Size that must be found and repaired: 0.1 micron
  - Number of such defects allowed: 0
  - Size ratio: defect to the mask area: size of a basketball area of California
- **Data**
  - Typical number of mask layers for 90 nm generation logic product: 22—25
  - Total file size needed to specify all these layers: 200 GB
  - Time to transmit (design site to mask shop) using T1 line (1.4 MB/sec): ~1.5 days
  - Time using T3 line (40 MB/sec): ~1.5 hours
- **Cost**
  - Cost to lease a T3 line: $70K/month
  - Capital cost to build a 90 nm node capable mask shop (capacity of 200 sets/year @50-70% yield): $200-250M
  - Yearly cost to operate such a shop: $60-100M
  - Cost to make a 90 nm node mask set (depreciation, labor, etc): ~$800K-1.3M

intel

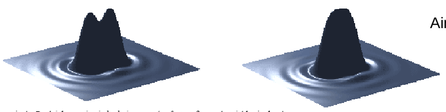
Litografia Imersyjna



$$W = \frac{k_1 \lambda}{NA}$$

Litografia Imersyjna

Zdolność rozdzielcza (kryterium Rayleigha)
W – najmniejszy rozmiar dostępny w litografi, mikroskopii etc.



Airy disks

The third element in the Rayleigh equation is k_1. k_1 is a complex factor of several variables in the photolithography process such as the quality of the photoresist and the use of resolution enhancement techniques such as phase shift masks, off-axis illumination and optical proximity correction. While exposure wavelengths have been falling and *NA* rising, k_1 has been falling as well, see figure 2. The practical lower limit for k_1 is thought to be >0.25.

$$NA = n \sin\alpha = d/(2f)$$

$$W = \frac{k_1 \lambda}{NA}$$

$$W = \frac{0.25 \times 193}{0.93} = 52nm$$

$$W = \frac{k_1 \lambda}{n \sin\alpha} = \frac{0.25 \times 193}{1.47 \times 0.93} = 35nm$$

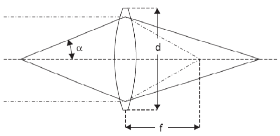
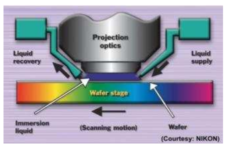


Figure 3. Numerical aperture.

Litografia Imersyjna



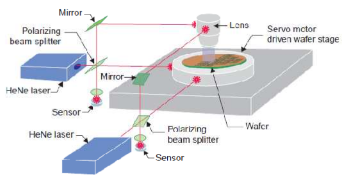
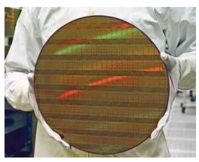


Figure 4. Stepping exposure system stage control



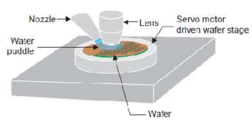
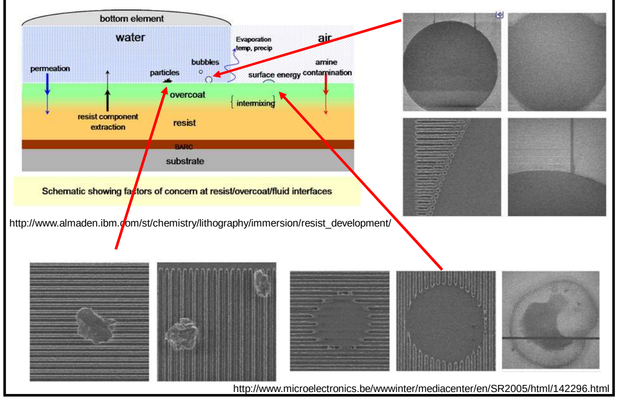


Figure 5. Immersion lithography. Stage control omitted for clarity.

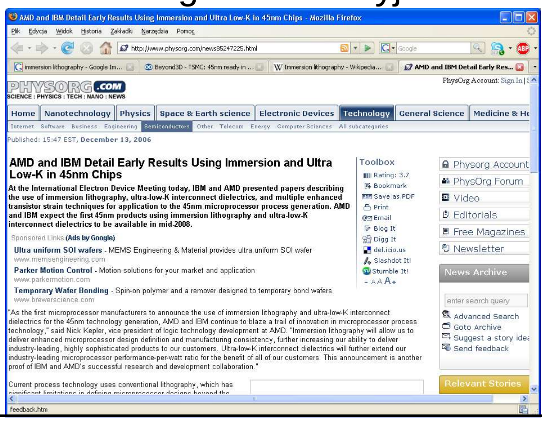
http://www.smalltimes.com/articles/stm_print_screen.cfm?ARTICLE_ID=260007

Litografia Imersyjna

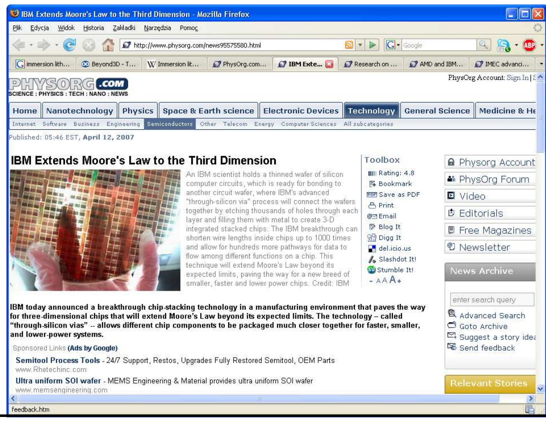


Litografia Imersyjna

Litografia Imersyjna



Inne



Stempelki

www.research.ibm.com/journal/rd/455/michel.html

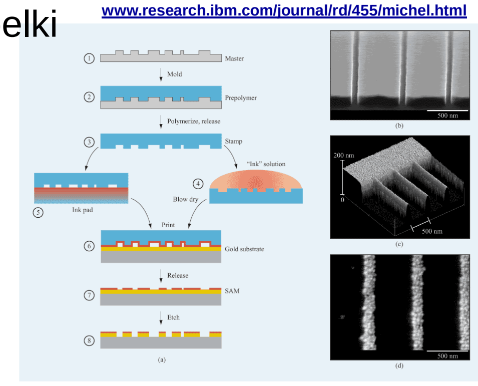
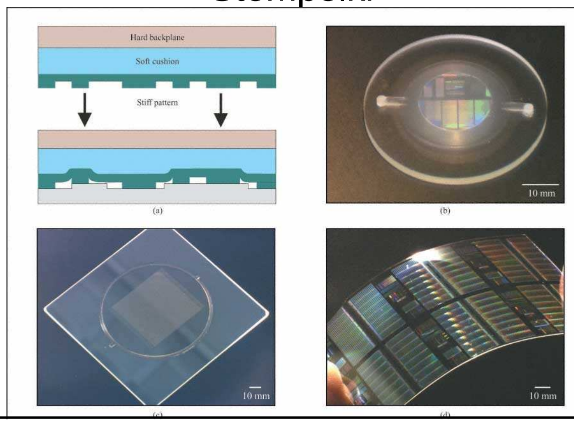


Figure 3

Soft-lithography components. (a) Diagram of process: A prepolymer (2) covering the master (1) is cured by heat or light, and demolded to form a elastomeric stamp (3). The stamp is inked by immersion (4) or contacted with an ink pad (5), and printed onto the substrate (6), forming a self assembled monolayer (SAM). The ink pattern (7) is then transferred into the substrate by a selective etch (8). (b) Scanning electron microscop (SEM) micrographs of the master, (c) image of the stamp, and (d) SEM micrograph of a printed and etched pattern.

Stempelki



Inne udoskonalenia

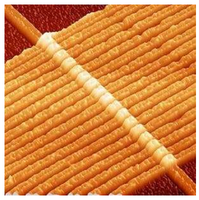
Uniwersytet Warszawski

Memrystor

The missing memristor found nature

Dmitri B. Strukov[1], Gregory S. Snider[1], Duncan R. Stewart[1] & R. Stanley Williams[1]

Vol 453 | 1 May 2008 | doi:10.1038/nature06932



"A memristor is essentially a resistor with memory," explains Stan Williams of HP Labs in Palo Alto, California, who reports the memristor's creation in this week's Nature. "The actual resistance of the memristor changes depending on the amount of voltage and the time for which that voltage has been applied to the device."

May 2008, Hewlett Packard

Uniwersytet Warszawski

Udoskonalenia

Physics of Semiconductors and their Heterostructures. Jasprit Singh

Strained Silicon

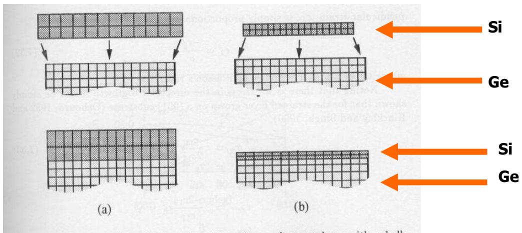
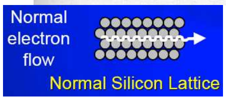
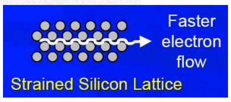


Figure 7.6: Pseudomorphic strain produced by epitaxy of an overlayer with a bulk lattice constant larger (a), or smaller (b) than the substrate. The overlayer must match the in-plane lattice constant of the substrate.





Udoskonalenia

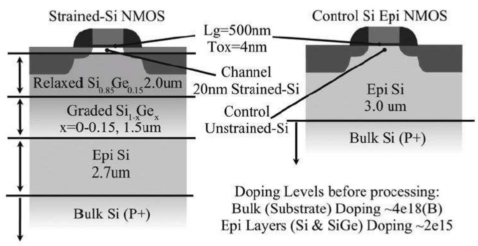


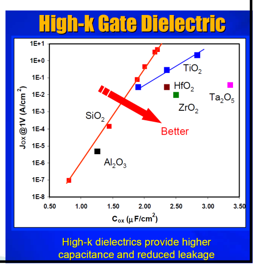
Fig. 1. Strained-Si and control Si nMOS structures.

Improved Hot-Electron Reliability in Strained-Si nMOS
David Onsongo, IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 51, NO. 12, DECEMBER 2004 2193

Udoskonalenia

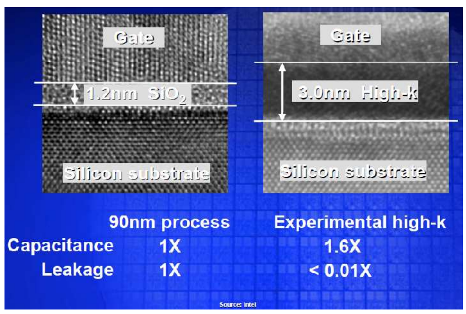
High-k dielectric material

- Pojemność: $C = S\,k / d$
- Stosowane by zminimalizować prąd tunelowy oraz dyfuzję boru z bramki
- Rodzaje:
  1) $4 < k < 10$; SiN_x
  2) $10 < k < 100$; Ta_2O_5, Al_2O_3, TiO_2
  3) $100 < k$



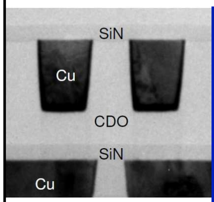
Udoskonalenia

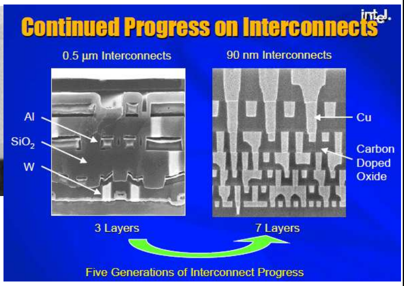
High-k dielectric material



Udoskonalenia

Low-k dielectric material

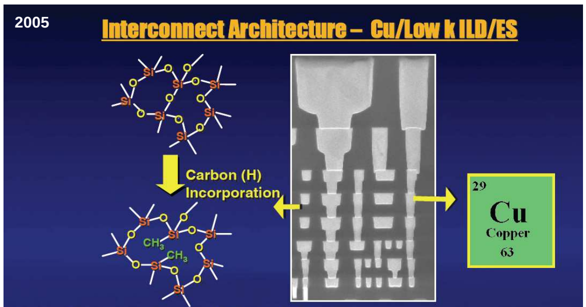




Carbon Doped Oxide
Redukcja pojemności o 25%

Project 4

Udoskonalenia



- 8 layers advanced Cu metallization
- 2nd generation CDO (Carbon Doped Oxide) low k ILD and etch stop layers for power reduction and RC improvement

Intel

Udoskonalenia - tranzystory

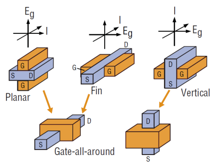


Figure 1. Double-gate to multigate CMOS structures [3]. E_g = gate field direction; I = channel current direction.

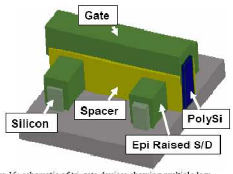


Figure 15: schematic of tri-gate devices showing multiple legs.

ftp://download.intel.com/technology/silicon/Chau%20DRC%20062303.pdf

Źródło: Intel

Tranzystory

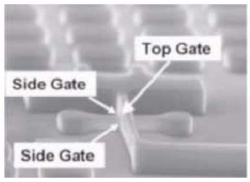


Figure 1. Photo of a 30-nm tri-gate transistor

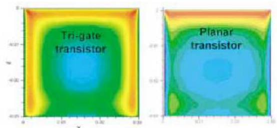


Figure 2. This simulation of a cross-section of silicon channel shows much more current flow (indicated by red) in a tri-gate transistor than in a planar transistor. Current flows into/out of the paper.

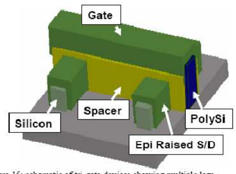
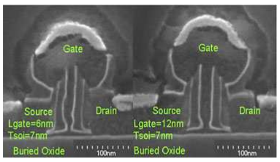


Figure 15: schematic of tri-gate devices showing multiple legs.

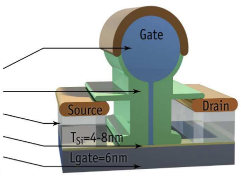
ftp://download.intel.com/technology/silicon/Chau%20DRC%20062303.pdf

Źródło: Intel

CMOS logic is holding on



Extreme Scaling with Ultra-thin Silicon Channel MOSFETs
Ieong et al. (IBM) IEDM 2002

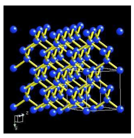


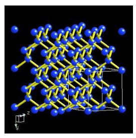
RSD stands for "Raised Source Drain"
Box stands for "Buried Oxide"

Source: IBM

David Williams *Hitachi-Cambridge*

Gdzie jest limit
Scaling problems



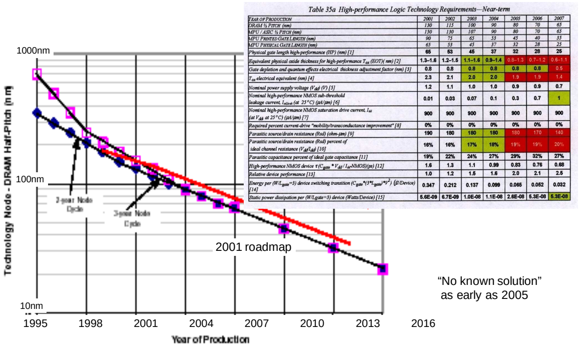


FEATURE	LIMIT	REASON
Oxide Thickness	2.3 nm	Leakage (I_{GATE})
Junction Depth	30 nm	Resistance (R_{SDE})
Channel Doping	V_T=0.25 V	Leakage (I_{OFF})
SDE Under Diffusion	15 nm	Resistance (R_{INV})
Channel Length	0.06µm	Leakage (I_{OFF})
Gate Length	0.10µm	Leakage (I_{OFF})

2003

SDE Source-Drain Extensions

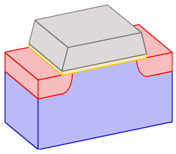
The ITRS Roadmap



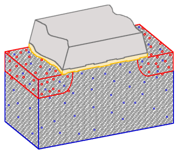
"No known solution" as early as 2005

David Williams *Hitachi-Cambridge*

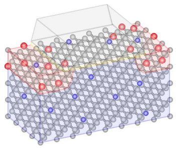
Granice miniaturyzacji?



Myślimy, że tranzystor jest zbudowany tak.



25 nm MOSFET
Produkcja od 2008



4,2 nm MOSFET
Produkcja ???

Asen Asenov, Glasgow
David Williams *Hitachi-Cambridge*

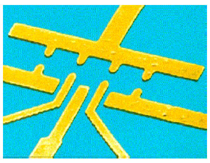
IEEE Trans Electron Dev 50(9), 1837 (2003)

Tranzystory

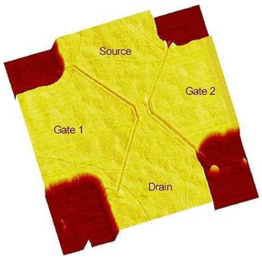
•About the figure:
•Figure taken from the Website of Leo Kouwenhoven from the Delft group, Delft, The Netherlands.
•Single-Electronics links
- **•Stony Brook/Likharev's group**
- **•Links via Stony Brook**
- **•Delft**

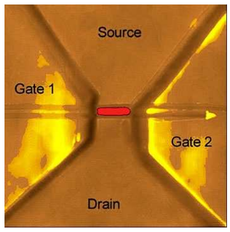
•NanoLinks

Programable logic



Tranzystory

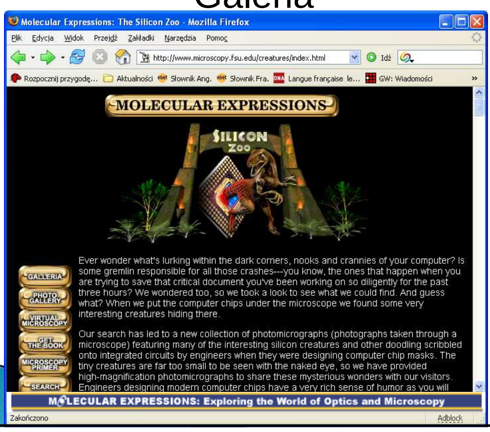




An in-plane gate (IPG) transistor made by scratching a semiconductor surface with the probe of a atomic force microscope (AFM). The scratches subtly influence the behavior of a layer of electrons trapped at a buried interface underneath the surface. The gap between the transistor's source and drain is one micron.

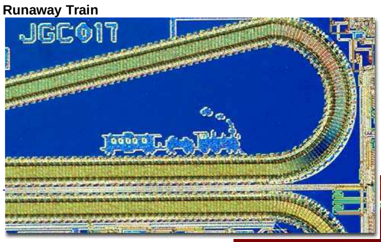
An AFM picture of a single-electron transistor (SET) made in the same way as the IPG transistor. The red region, the island where only single electrons may be admitted, measures 100 x 200 nm. reported by: Schumacher et al., in the 23 August *Applied Physics Letters*

Galeria



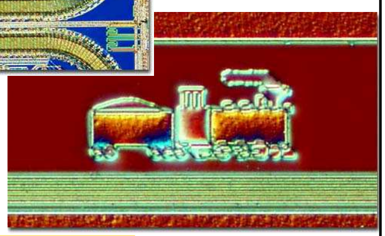
Galeria

Runaway Train



We ran into this miniature locomotive at a railroad crossing on an Allen-Bradley/VLSI standalone ASIC that was fabricated in 1994. Bob Weppler, designer of the train, has informed us that he placed the locomotive and coal car on the chip at the request of engineer Jerome Saint-Cyr to represent "the little engine that could". This was in reference to the fact that the chip has a small RISC core microprocessor allowing it to compete with its more advanced counterparts. Bob says that the locomotive was fabricated in two metal and one polysilicon layers during the chip's manufacturing process.

"The Little Engine That Could"



This miniature choo-choo train was discovered rolling down the tracks on a LeCroy MVV 200 analog shift register integrated circuit. The existence of the train was brought to our attention by John T. Anderson of JPS Designs located in Elburn, Illinois. The "tracks" upon which the train is apparently riding are the high speed shift register. This chip is based on Charge Coupled Device (**CCD**) technology, where analog samples of electrical charge are temporarily stored in the chevron-shaped tracks, and control signals create electrical fields that "bump" the charge along from segment to segment.

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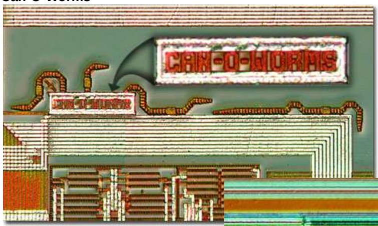
http://www.microscopy.fsu.edu/creatures/index.html

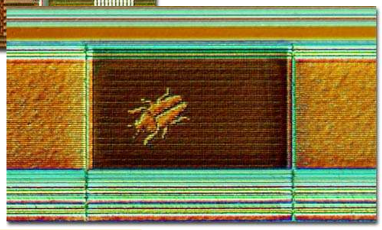
Galeria

Can-O-Worms



We've Got Roaches

The term "computer bugs" arose earlier in the century when insects were discovered to be the cause of malfunctions in the relays used in very early computers. In some cases, the bugs would induce a short-circuit by getting caught in the mechanical relay contacts and would have to be removed manually. As progress would have it, we must now deal with silicon insects as evidenced by the photomicrograph of a roach that we captured scurrying across the surface of a Hewlett-Packard CPU support chip. So far, this is the only silicon bug we have found, but we're keeping our eyes peeled.
The photograph below contains a page from the 1945 logbook of the Mark I computer at Harvard University, one of the first computers ever built. Engineer Grace Murray Hopper and her associates were testing the Mark I one day when the machine suddenly stopped. Upon inspection, they found a fried moth that had become wedged into one of the relays, causing a short circuit and halting the computer. Hopper taped the bug into her logbook (illustrated below), and we have been referring to computer glitches as "bugs" ever since.



The can of worms illustrated in the digital image presented above is the creation of designer Greg Rohde, who placed the doodle on the Lattice Semiconductor Corporation's popular **ispPAC30** integrated circuit to symbolize the numerous problems encountered during the design. Often, these problems required one of the circuit engineers to "open up another can of worms" to solve design problems. The chip contains a total of four programmable gain instrumentation amplifiers, two multiplying digital-to-analog converters, and two configurable output amplifiers with rail-to-rail outputs.
There are two additional doodles on the **ispPAC30** integrated circuit. One is a pack rat (general logo for the design team), while the other is a wolf silhouette, which is the signature of Reo Gargovich, the lead designer on this chip.

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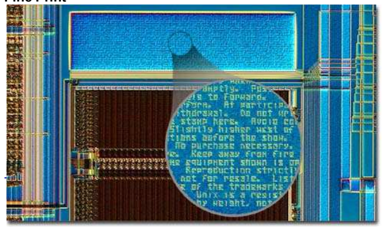
Galeria

Fine Print



This is undoubtedly the most surprising doodle that we have ever discovered adorning the surface of an integrated circuit. Most people are used to seeing warranty disclaimers on everything from refrigerators to software, but this is the first one we have encountered on a silicon chip. Our hieroglyphics experts have not yet deciphered the entire body of text, but the phrases "No purchase necessary", "Keep away from fire", and "not for resale" are clearly visible in the magnified portion shown as an inset within the photomicrograph. The pad containing this warranty is 450 microns tall by 1850 microns wide and sports 25 lines of text, with each character being between six and eight microns high. This disclaimer--probably the smallest ever written--was found on a Hewlett-Packard "Aspen" (**A**cquisition **S**ignal **P**rocessing **EN**gine) chip used in digital oscilloscopes in the late 1980s and early 1990s.

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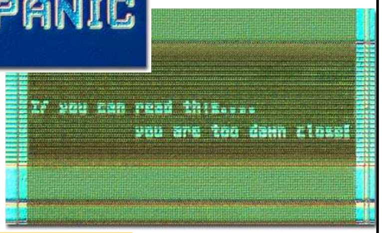
Galeria

Don't Panic

We stumbled across this 5 micron-high phrase while examining the surface of a Hewlett-Packard Pit Viper memory controller chip. As the saying goes: If you can read this....you are too damn close! When we saw it, we backed off a little bit, took the photograph, then split (we don't have to be warned twice).

Too Damn Close!



Don't Panic - when uncertain about your whereabouts in the Universe or the strange customs of new aliens that might cross your path. Just consult your guidebook: "The Hitchhiker's Guide to the Galaxy", where you will find that the number 42 is the answer to the question about life and the universe. Or so says a supercomputer named "Deep Thought". We've been stuck on planet Earth these past few decades so our information about the phenomenon is incomplete.
These science fiction symbols were discovered on a node adapter chip that serves as an interface between a remote I/O link and a microprocessor-based product, developed by Allen-Bradley/Rockwell in 1988. Chip designer Bob Weppler tells us that these icons from the famous Douglas Adams sci-fi novel were included on the chip along with the cricket wicket and a Sperm whale that slammed into the planet Magrathea.

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Galeria

This Bird's For You

This is a very high magnification view of what appears to be a hummingbird etched into the silicon on a Hewlett-Packard PA-RISC 7000-series microprocessor wafer. The inscription above the bird reads: "This Bird's For You", but we don't think that it is for us. We think that it is for you.

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Galeria

Thor: God of Thunder

This magnificent rendition of Thor, the Norse god of thunder, was discovered on a Hewlett-Packard graphics support chip. According to legend, Thor was the son of Odin and Jord and later married Sif (a fertility goddess), although he kept a mistress named Jarnsaxa (the "iron cutlass"). It was also widely believed that during a thunderstorm, Thor could be found sailing through the heavens on his goat-powered chariot, and that lightning flashed whenever he threw his hammer (named Mjollnir).
At 1.1 square millimeters in size, this silicon artwork is not only the finest we have seen to date, it is also one of the largest and required our lowest-power microscope objective (5x) to capture the entire image. Hewlett-Packard engineer Rick Butler loaned us this chip, along with the marathon chip that contains a tennis shoe. Rick was also instrumental in providing us with information about the "sunken via" method of creating these doodles as revealed in our interactive Java tutorial on building a silicon Yin Yang, and other general discussions about silicon artwork.
Hewlett-Packard chip designer Darrin Miller originally decided to incorporate the Thor rendition on this chip. He asked graphics designer April Comer to draw the Viking and she produced four ideas about how the god could appear. Darrin picked one and turned it into a contact "bitmap" for placement on the final masks, yielding the image presented above. It is somewhat ironic that both Darrin and April are graduates of the University of Florida, our in-state football rivals.

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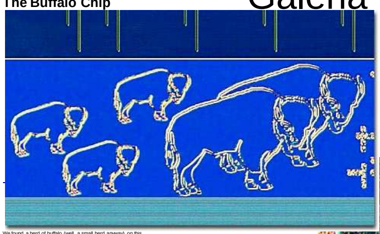
Galeria

The Buffalo Chip



We found a herd of buffalo (well, a small herd anyway) on this Hewlett-Packard 64-bit combinatorial divider, the Focus II Math chip. We don't know the significance of these bison-like silicon creatures, but they are some of the coolest buffalo that we have seen. One suggestion about the buffalo, which we feel is worth mentioning, was brought to our attention by Travis Thomas of Austin, Texas. Travis is under the opinion that the significance of the bison is to denote "buffalo chips", of which these are certainly one form. In fact, Travis' suggestion led us to change the title of this gallery entry.
The herd of buffalo was devised and executed onto the chip by HP engineer Dick Vlach, who tells us that the buffalo are dividing and leaving chips behind. John Carlson was the chief design engineer for this chip, and Dan Zuras is responsible for the crossword puzzle of designers' names that appears directly to the right of the buffalo (only a small portion of the puzzle is visible in this photomicrograph). This chip was designed by the Fort Collins, Colorado HP chip design team and the buffalo are a mascot of the nearby school, the University of Colorado.

I Love Hewlett-Packard

We discovered this tiny heart on the Hewlett-Packard buffalo chip loaned to us by Jon Singer of the Joss Research Institute. It looks like the chip designers had a thing for Hewlett-Packard.

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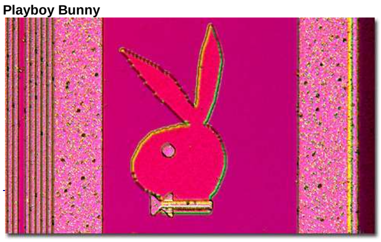
Galeria

Playboy Bunny



One of America's favorite icons, the Playboy bunny, was discovered on an integrated circuit made in Germany by Siemens. The bunny rabbit head logo was originally designed by Art Paul, the first art director of Playboy Magazine, and has appeared on the cover of every issue (with the exception of the very first). Hugh Hefner, creator of the concept is quoted:

"I selected a rabbit as the symbol for the magazine because.... he offered an image that was frisky and playful. I put him in a tuxedo to add the idea of sophistication. There was another editorial consideration, too. Since both the '*New Yorker*' and '*Esquire*' use men as their symbols, I felt the rabbit would be distinctive; and the notion of a rabbit dressed up in formal evening attire struck me as charming, amusing, and right."

The integrated circuit was donated to the Silicon Zoo by German photographer Karl E. Deckart, who is one of our featured microscopists. To view more of Karl's work, visit his **Mikro/Makro** website, which contains a sampler of his transmitted and reflected light images captured with a microscope.

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Galeria

The Cheetah

We captured this beautiful cheetah racing across the surface of a Hewlett-Packard memory controller integrated circuit. The chip was designed in combination with a very early HP-PA microprocessor that was code named Cheetah and used in the HP-900/750/755 series computers. Cupertino engineer Willy McAllister originally found the image on the cover of the September 1986 IEEE Computer magazine and asked his wife, Monica (a graphics artist), to redraw the image for placement on the chip. The redrawn cheetah was digitized by Dick Vlach, one of HP's top mask designers, and incorporated into the mask--and subsequently onto silicon.

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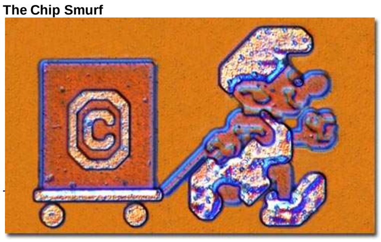
Galeria

The Chip Smurf



We caught this silicon Smurf pulling a wagon containing the copyright symbol around the pad ring on a Siemens integrated circuit of unknown function (the M879-A3). Like other Smurfs, this figurine was originally created by Belgian cartoonist Pierre Culliford (also known as Peyo), and introduced into the United States in the late 1970s. In the early 1980s, the Smurf culture exploded when the National Broadcasting Company (NBC) launched a cartoon series featuring the tiny creatures. Smurfs typically are blue, wear white hats, and stand three apples high. This guy goes against the grain with his orange skin and yellow hat. In addition, he is only about 60 micrometers high, more than 1000 times smaller than a single apple.

The photomicrograph was donated to the Silicon Zoo by German photographer Karl E. Deckart, who is one of our featured microscopists. To view more of Karl's work, visit his **Mikro/Makro** website, which contains a sampler of his transmitted and reflected light images captured with a microscope.

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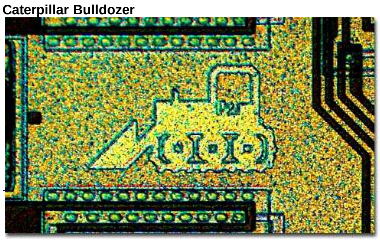
Galeria

Caterpillar Bulldozer



This miniature rendition of a bulldozer appears on a NMOS digital chip designed in 1980 for Caterpillar by Synertek for use in their heavy equipment Electronic Monitoring Systems. The integrated circuit is still used in many models of Caterpillar construction equipment, including bulldozers. We suspect that the bulldozer is busy clearing space on the chip for additional transistors. The chip was loaned to us by Chuck A. Morrill, a Semiconductor Component Engineer who conducts failure analysis testing and sourcing of chips for electronic controls at Caterpillar. Now, ain't this slick?

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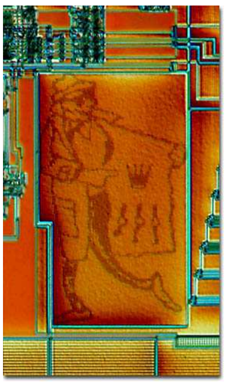
Galeria



The Con Artist

We found this interesting creature on the Hewlett-Packard superscalar PA-RISC 7100LC Hummingbird microprocessor chip not far from the hummingbird (you know---the one that is for you). The guy with the sunglasses appears to be showing a number of items, including some (probably) "hot" watches, inside his trench coat. From the crown advertisement on the inside of his coat, we think that this guy expects us to believe they are genuine Rolex watches. Although we don't understand the significance of this scam artist or whom he expects to con while lurking around on this chip, he is one of our most unusual busts to date. It's characters like this that lead us to suspect that a secret cartoon culture is being perpetuated on hidden silicon. Several emails from HP engineers Patrick Knebel, Wayne Kever, Craig Robson, and Bob Miller have cleared up the mystery of this con artist. Early HP chipsets included a separate floating-point math coprocessor, and the HP-9000/720 workstations used a Texas Instruments chip that was termed the "Timex" coprocessor. In later microprocessors, HP integrated the floating-point unit onto the CPU die. The PA-7100 microprocessor contains the "Rolex" floating-point circuitry integrated onto the chip, and this advanced circuitry features greater performance than the Timex coprocessor. The clock circuitry was later redesigned to save space (modestly reducing double-precision performance) on the PA-7100LC (Low Cost) processor and the floating point array was then nicknamed "Lorex", a pun on the low-end Rolex. The con artist (designed by HP VLSI design engineer Bob Miller) was placed on the PA-7100LC with a modified Rolex crown that is missing a point (it only has four), to symbolize the cheap Rolex knock-offs, "Lorexes" that he is apparently trying to pawn.

Another interesting feature of the con artist is the unusual way this creature was created on the chip. The vast majority of silicon creatures are created as "wireframe" metal layers on a silicon dioxide surface. The con artist was constructed in a series of small squares, much like a bitmap image. The technique using these small squares is the safest technique that engineers have for patterning these miniature doodlings. The actual squares are really contacts (voids where a hole is produced in the dielectric medium) between two metal layers and appear as a series of slight dents in the surface of the chip. This is demonstrated with our **Yin Yang interactive Java tutorial** that illustrates how these doodles are formed on the surface of an integrated circuit.

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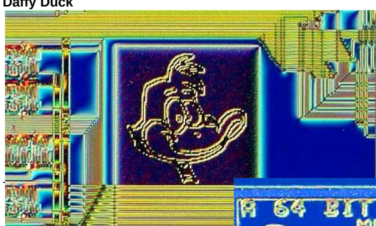
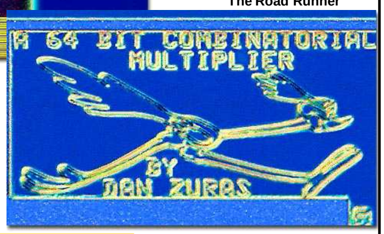
Galeria

Daffy Duck



The Road Runner Show, a 30-minute cartoon series, premiered on the CBS television network on September 10, 1966. The episodes featured three cartoons, one with the Road Runner and Wile E. Coyote (whom we have never found on a chip), and two with other Warner Brothers cartoon characters. The Road Runner cartoons featured humorous scenarios in which the Road Runner would out-smart the rather dumb coyote and usually cause him serious cartoon injuries. We found this version of the Road Runner on a Hewlett-Packard 64-bit combinatorial multiplier integrated circuit. The major design credit is given to Dan Zuras, whose name appears just below the Road Runner.

The Road Runner



As we see it, the engineers that designed this wireframe version of Daffy Duck must have had a very interesting sense of humor. We found it deeply embedded within the circuitry of a RISC microprocessor, about 1500 microns away from a similar-style rendition of Waldo. Daffy is about 50 microns in size, making it necessary to use a high-power (40X to 60X) microscope objective to photograph the wireframe character.

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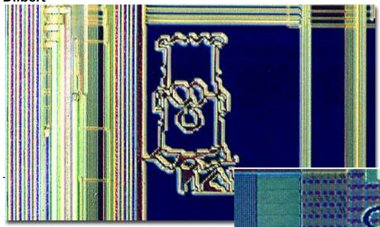
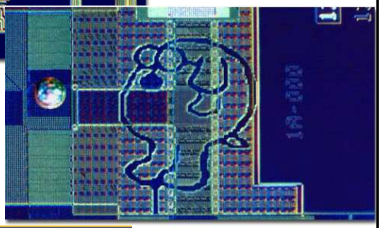
Galeria

Dilbert



From the Scott Adams cartoon strip, we present this photomicrograph of cyber-engineer Dilbert, caught hiding from his omnipresent boss within the circuitry of a computer chip. Dilbert, voted by his high school classmates as "Most likely to find a potato that resembles himself", is one of our favorite cartoon characters.

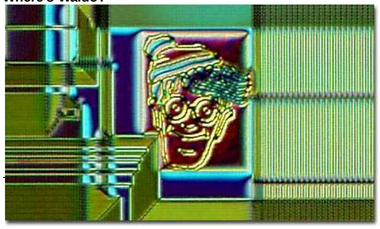
Dogbert



One of today's most popular cartoon strips is **Dilbert**, written by Scott Adams and syndicated by every major newspaper in the United States. We have found two of the main characters in this comic strip, Dilbert and Dogbert, on the two biggest and fastest microprocessors in our collection. This silicon version of the Dogbert character, as illustrated above, is about 140 microns in size.

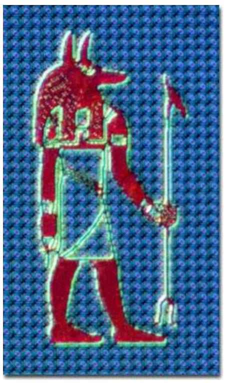
Galeria

Where's Waldo?



Just about everyone we know has spent time searching for Waldo in the comic strips (and we have too!). The photomicrograph above illustrates a wireframe rendition of Waldo that we found hiding on the surface of a microprocessor integrated circuit. Discovering this version of Waldo proved to be much more difficult than the one in the comics. When searching the Sunday comic strip, you have to screen several hundred faces to find the real Waldo hiding, usually in a crowd, behind a building or in a corner. We caught this silicon version of Waldo (that is about 30 microns in size) hiding among caches, buses, and registers while searching through many thousands of square microns of complex circuitry with a high-power optical microscope. Waldo is the first Silicon Creature that we discovered, and this led to an exhaustive search for more creatures and construction of the Silicon Zoo gallery.

Galeria

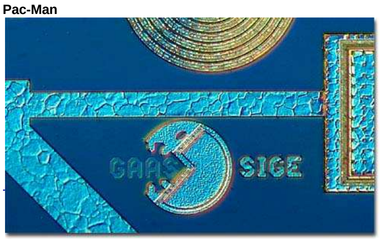


Ancient Egyptian God Anubis

While examining the Silicon Graphics MIPS R12000 microprocessor, we found a pair of Egyptian gods that appear to be guarding mask alignment targets on the chip. The photomicrograph above depicts one of the figures who we think is a representation of Anubis, a Jackal-headed Egyptian god who was in charge of embalming and mummification of the royal deceased. This creature is about 100 microns high.

Galeria

Pac-Man



We spotted this silicon Pac-Man gobbling the initials GAAS (gallium arsenide) on a TEMIC Semiconductors silicon-germanium radio frequency integrated circuit. This chip is the first Digital Enhanced Cordless Telecommunications (DECT) device produced with silicon-germanium technology, replacing the usual gallium arsenide power amplifier devices normally used in DECT applications. Similar devices made using gallium arsenide are expensive and normally require a negative auxiliary voltage. We assume the Pac-Man silicon icon was planted on the chip as a symbolic gesture to the fact that devices made with silicon-germanium are poised to "eat up" the gallium arsenide-based competition.

Pac-Man was originally designed by Toru Iwantani and programmed by Hideyuki Mokajima and his associates. The name Pac-Man is derived from the Japanese slang "**Paku-paku**", which means "**to eat**". Originally, the Japanese named the game "**Puckman**", but it was changed to "**Pac-Man**" upon launching in the United States. Pac-Man is the best-selling video arcade game in history, and the yellow gobbling Pac is probably the most recognized video character. The game has spawned a number of side products including cartoons, lunch boxes, board games, clothing, and numerous other products.

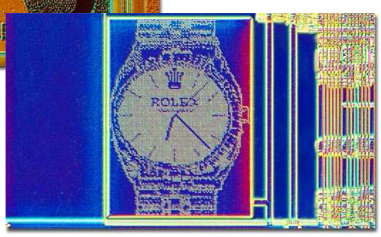
The chip containing this artwork was loaned to us by **Chipworks**, a company that is an international provider of reverse engineering services, analyzing the circuitry and physical composition of semiconductor chips and electronics systems for competitive study, intellectual property support, and reliability assurance.

Galeria

The Pepsi Generation

This incredible rendition of a Rolex wristwatch was discovered nested within the clock circuitry of a Hewlett-Packard PA-7100 microprocessor, the chip code named ***Thunderbird*** that also contains **The Bird is the Word** entry in the Silicon Zoo. The Rolex is another example of the ingenious **Sunken Via** method of constructing doodles using a bitmap of via shafts developed by HP chip designers in Fort Collins, Colorado. This method of constructing silicon creatures is based on the formation of images through patterns (a series of tiny squares), much like bitmap images are composed of a series of pixels, where each covered via shaft represents an individual pixel. The Rolex is made with over 5000 individual via shafts. Other entries in the gallery constructed in the same manner include: **The Con Artist**, **This Bird's For You**, **The Sundial**, and **The Thunderbird**. Additional information about the evolution of silicon doodles within HP microprocessor clock circuitry can be found in text accompanying the **Con Artist** gallery entry.

The Rolex

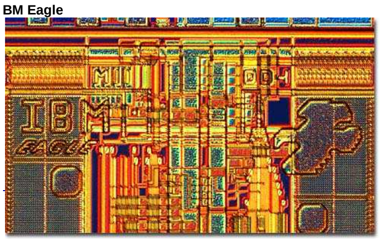


Do you remember when a bottle of Pepsi cost a nickel? We can't either, so we did a little research to find out the approximate date of what is undoubtedly the smallest advertising sign yet created (the silicon rendition featured above--about 750 microns wide). Pepsi-Cola was first introduced as a fountain drink in 1898, prior to the widespread use of bottled soft drinks. A few years later, Caleb Bradham began bottling Pepsi in a plant located in New Bern, North Carolina. After the great depression, advertising emphasis was shifted to low cost and high product value. In 1934, Pepsi-Cola became the first soft drink manufacturer to replace the popular six-ounce bottle with a 12 ounce bottle for a nickel. This was widely advertised in signage of the period, as illustrated with the authentic reproduction done in silicon above. We found this sign on a Hewlett-Packard CPU-support integrated circuit. The arrow, difficult to read at this magnification, contains the text: "Look for the Trade Mark", and the bottom of the label reads: "Healthful" (thank god the FDA wasn't around!) and "Refreshing".

The Hewlett-Packard integrated circuit featuring this tiny silicon rendition of a Pepsi commercial was donated to us by HP chip designer Craig Robson, who designed the artwork.

Galeria

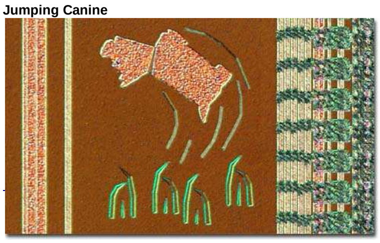
BM Eagle



We were notified about the existence of this eagle by John Deters, who loaned us a copy of the chip for digital imaging through the microscope. The artwork was placed on a very early version of a 1 Mb memory chip made by IBM in the mid-1980s. Because the integrated circuit used older 256 Kb technology, it was larger and slower than later 1 Mb chip designs. However, the chip was a significant cost improvement over existing 256 Kb chips of the period and enabled IBM to compete more effectively with Japanese 64 Kb chips that were selling at 1/20th the cost. Featured on the chip is the image of a bald eagle (designed by engineer Scott Lewis), which overlaps into a cache region of the chip. Also present, on the left-hand side of the image, are the letters IBM and the designation "Eagle", which is probably the code-name for this random access memory integrated circuit.

Galeria

Jumping Canine

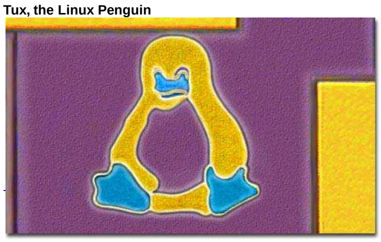


We discovered this somersaulting canine on a Digital VAX microprocessor support chip loaned to us by designer Bob Supnik. There appears to be clumps of silicon "grass" below the dog and he seems to be having a good time (probably happy that this chip design finally made it into silicon).

MOLECULAR EXPRESSIONS: Exploring the World of Optics and Microscopy http://www.microscopy.fsu.edu/creatures/index.html

Galeria

Tux, the Linux Penguin



A chip designer informed us of a miniature replica of Tux, the Linux penguin nesting in the pad ring of an integrated circuit of unknown type and function. If we obtain more information about the chip, it will be posted (maybe it's a special microprocessor that is optimized for the operating system). Linus Torvalds, creator of the Linux operating system, was the one who originally had the idea for a penguin as the Linux logo "center"piece. The cute little penguin rendition illustrated above measures about 130 microns in size.

MOLECULAR EXPRESSIONS: Exploring the World of Optics and Microscopy http://www.microscopy.fsu.edu/creatures/index.html

Galeria

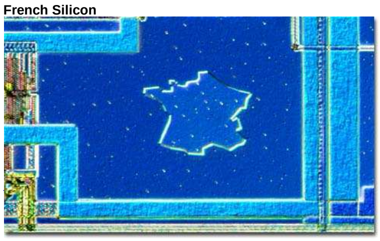
The Wedding Announcement

This unusual wedding announcement appears on the Silicon Graphics MIPS R10000 microprocessor. The inscription reads: Ellen & Yeuk-Hai, May 25, 1996 and we are told that the announcement is for the wedding of a MIPS design engineer who supervised the development of masks for this microprocessor. The size of the announcement is approximately 100 microns. We were given a copy of the original photograph (courtesy of Yeuk-Hai Shark Mok) from which the wedding announcement was derived, and this is displayed below for comparison purposes.

MOLECULAR EXPRESSIONS: Exploring the World of Optics and Microscopy http://www.microscopy.fsu.edu/creatures/index.html

Galeria

French Silicon

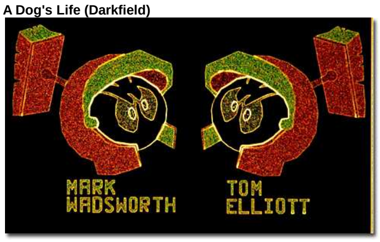


We were examining a Random Access Memory (RAM) integrated circuit manufactured by a partnership between Thomson and Mostek when we discovered maps of France and the state of Texas. The photomicrograph above depicts the map of France as seen on the chip. The tiny "bumps" on and surrounding the map do not designate cities in France---they are small particles of dirt incorporated into the circuitry during manufacture of the chip.

MOLECULAR EXPRESSIONS: Exploring the World of Optics and Microscopy http://www.microscopy.fsu.edu/creatures/index.html

Galeria

A Dog's Life (Darkfield)

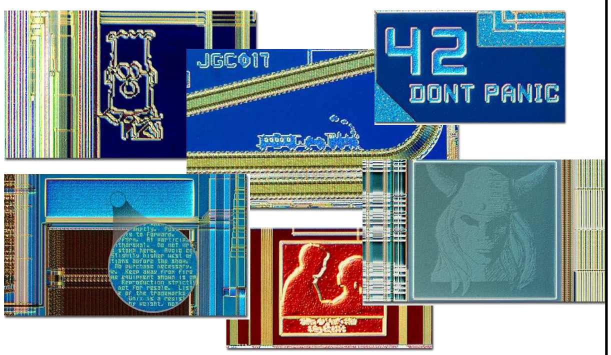


We managed to capture a photograph of what are now perhaps the tiniest Martians on Mars. Appearing as an opposed duet of helmeted gladiators, these angry silicon soldiers were discovered on the surface of an image sensor used by the **Spirit** and **Opportunity** rovers sent to probe the Red planet. Maybe these are the **ONLY** Martians on Mars? Probably not. In any event, the chip was loaned to us by designer Mark Wadsworth who is a fan of the Silicon Zoo. Mark informs us that he decided to try his hand at silicon artwork after visiting the Zoo on several occasions. The title of his artwork is the "Dueling Marvin the Martians". Mark designed the image sensor for NASA's Jet Propulsion Laboratory along with Tom Elliot, who actually did the testing of the flight candidate imagers to select the 20 or so that actually made it on the two missions. Tom and Mark tended to butt heads quite a bit, which was the inspiration for the doodle.

The rover image sensors are charge-coupled devices (**CCDs**) much like those found in ordinary everyday digital cameras, but with several advanced features. In order to speed image capture, the CCD uses frame transfer technology to quickly shift the captured image behind a mask (the **shielded region** electronic shutter in the image below) after the **photodiodes** have accumulated sufficient charge (relating to the image intensity). This particular sensor contains 1024 x 1024 pixels, each of which is 12-micrometers square. The chip is a custom design that was developed to meet the rather stringent performance criteria cooked up by the mission's brainchild (Dr. S. Squyers) and his group at Cornell University.

MOLECULAR EXPRESSIONS: Exploring the World of Optics and Microscopy http://www.microscopy.fsu.edu/creatures/index.html

Galeria

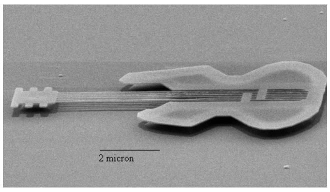


Hewlett-Packard, Allen-Bradley, LeCroy, Lattice Semiconductor Corporation, Siemens, Caterpillar, Silicon Graphics, TEMIC Semiconductors, IBM, Digital VAX, Thomson...

MOLECULAR EXPRESSIONS: Exploring the World of Optics and Microscopy http://www.microscopy.fsu.edu/creatures/index.html

Litografia 3D

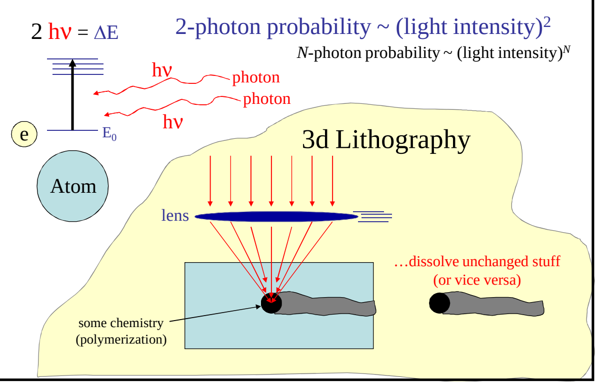
Lasery ekscymerowe



Electron-microscope image of the world's smallest guitar, based roughly on the design for the Fender Stratocaster, a popular electric guitar. Its length is 10 millionths of a meter-- approximately the size of a red blood cell and about 1/20th the width of a single human hair. Its strings have a width of about 50 billionths of a meter (the size of approximately 100 atoms). Plucking the tiny strings would produce a high-pitched sound at the inaudible frequency of approximately 10 megahertz. Made by Cornell researchers with a single silicon crystal, this tiny guitar is a playful example of nanotechnology, in which scientists are building machines and structures on the scale of billionths of a meter to perform useful technological functions and study processes at the submicroscopic level.
(Image courtesy Dustin W. Carr and Harold G. Craighead, Cornell.)

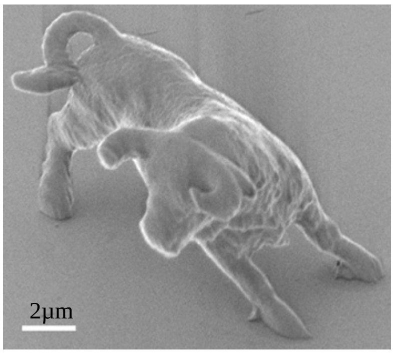
Litografia 3D

Photonic Crystals:Periodic Surprises in Electromagnetism Steven G. Johnson MIT



Litografia 3D

[S. Kawata *et al.*, *Nature* **412**, 697 (2001)]



λ = 780nm

resolution = 150nm

7μm

(3 hours to make)

Czego/kogo brakuje w Polsce

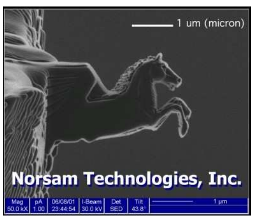
Uniwersytet Warszawski

Badania na Hożej

Focus Ion Beam

JEM-9320 Focused Ion Beam System

Dr Marta Gryglas
Dr Agata Drabińska



http://www.norsam.com/

Badania na Hożej

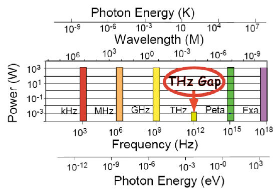
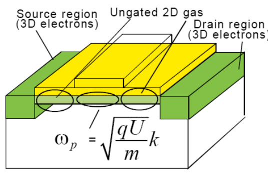


Fig. 1. "Terahertz gap"

Terahertz technology: devices and applications

Michael Shur

Dr Jerzy Łusakowski,
Dr Krzysztof Karpierz,
Mgr Maciej Sakowicz,
Prof. dr hab Marian Grynberg

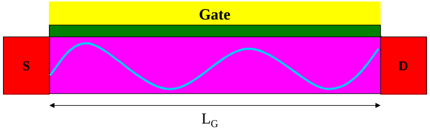


$$\omega_p = \sqrt{\frac{qU}{m}}k$$

Fig. 17. Frequencies of plasma oscillations, ω_p, versus wave vector, k, in a field effect transistor. m is electron effective mass, N is bulk electron concentration for alloyed regions, and n is sheet electron density for channel regions. (After [32].)

Badania na Hożej

Dr Jerzy Łusakowski,
Dr Krzysztof Karpierz,
Mgr Maciej Sakowicz,
Prof. dr hab Marian Grynberg



$$f_0 = \frac{1}{4L_G}\sqrt{\frac{e\cdot(U_{GS}-U_{TH})}{m}}$$

L_G = 100 nm
U_{GS} - U_{TH} = 1 V
m_e = 0.067 m_0

$\Rightarrow f_0 = 4THz$

GaAs

Badania na Hożej

Fig. 5 Application of a sub-THz technology for hidden weapon detection (from [4])

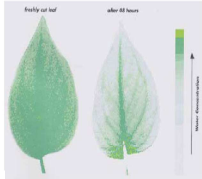


Fig. 4. THz images of a fresh leaf and the same leaf after 48 hours. Courtesy of TeraView, Ltd.

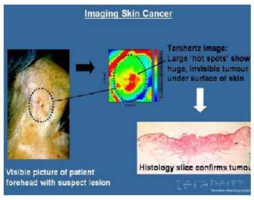
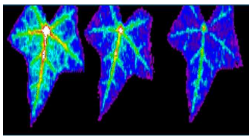


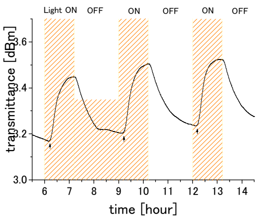
Fig. 3. Imaging skin cancer [3]. Courtesy of TeraView, Ltd.

Terahertz technology: devices and applications

Agriculture and Food Industry



Water contents of plants



Monitoring of plants

Wojciech Knap, CNRS

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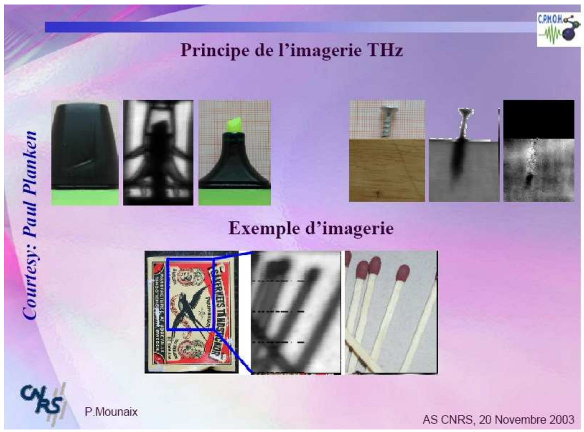


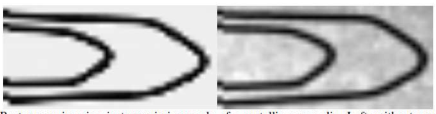


Fig. 11. Raster-scan imaging in transmission mode of a metallic paper clip. Left: without envelope, right: in envelope. 20 mm x 10 mm THz image was made with a numerical aperture of 0.5 and 0.3 mm pixel size (after Ref. 48).

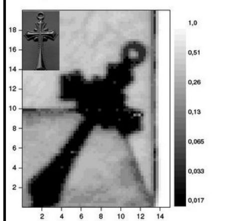


Fig. 10. b) The THz image of a metallic cross at 1.63 THz concealed in a paper envelope. Inset shows a photo of the cross for comparison. Scales are in millimeters, linear intensity scale is given in relative units.

J Infrared Milli Terahz Waves (2009) 30:1319–1337
DOI 10.1007/s10762-009-9564-9

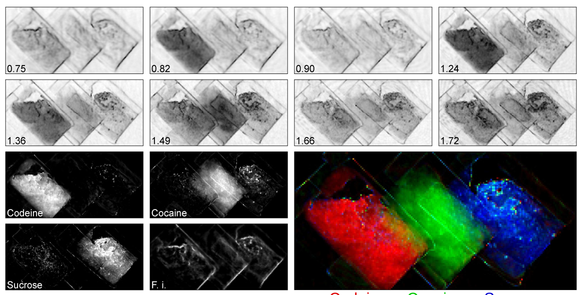
Field Effect Transistors for Terahertz Detection: Physics and First Imaging Applications

Wojciech Knap · Mikhail Dyakonov · Dominique Coquillat · Frederic Teppe · Nina Dyakonova · Jerzy Łusakowski · Krzysztof Karpierz · Maciej Sakowicz · Gintaras Valusis · Dalius Seliuta · Irmantas Kasalynas · Abdelouahad El Fatimy · Y. M. Meziani · Taiichi Otsuji

inżynieria nanostruktur

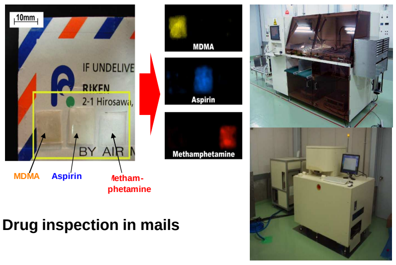
WYDZIAŁ FIZYKI UNIWERSYTET WARSZAWSKI

Chemical imaging



Wojciech Knap, CNRS

Narita – Japan Airport



Drug inspection in mails

Wojciech Knap, CNRS 121

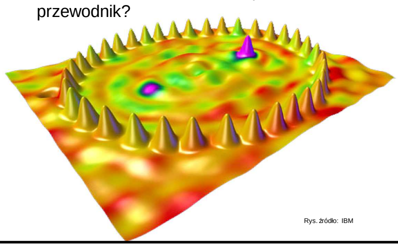
Nanotechnologia

Some Mask-Making Metrics and Comparisons

•Pixels:	
–On a 90 nm technology node mask:	1,000,000,000,000
–In a high quality digital photo:	4,000,000
•Defects:	
–Size that must be found and repaired	0.1 micron
–Number of such defects allowed:	0
–Size ratio: defect to the mask area:	size of a basketball area of California
•Data	
–Typical number of mask layers for 90 nm generation logic product:	22—25
–Total file size needed to specify all these layers:	200 GB
–Time to transmit (design site to mask shop) using T1 line (1.4 MB/sec):	~1.5 days
–Time using T3 line (40 MB/sec):	~1.5 hours
•Cost	
–Cost to lease a T3 line:	$70K/month
–Capital cost to build a 90 nm node capable mask shop (capacity of 200 sets/year @50-70% yield):	$200-250M
–Yearly cost to operate such a shop:	$60-100M
–Cost to make a 90 nm node mask set (depreciation, labor, etc):	~$800K-1.3M

W następnym tygodniu
Kwanty, stany, pasma
mechanika kwantowa dla początkujących

1. Trochę historii
2. Świat klasyczny i kwantowy
3. Czy dwa półprzewodniki dają cały przewodnik?



Rys. źródło: IBM